

3상 PFC 위한 설계 고찰

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단일 위상 PFC(Power Factor Correction)시스템과 더불어 3상 위상 전력 시스템의 전압을 추적하는 전류 파형에 대한 필요가 2차적인 요구조건을 이끌어 낸다. 높은 역률(전류 파형은 전압 파형을 추적)을 필요로 하는 3상 위상 이외에도, 각 위상에서 소비되는 전력이 동일해야 한다는 또 다른 요건이 존재하고 있다.

이 기사에서는 이러한 기능을 제공하는 방법에 대해 논의하고자 한다. 또한, 각각의 필수 요소를 설계하는 방법에 대해 더 많은 자료를 제공할 것이다.

그림 1은 각각의 위상과 관련된 3상의 각 단계에서 전압과의 관계를 보여준다. 위상 0은 가장 두꺼운(붉은색) 선이다. 위상 1(검은색)은 120도까지 위상 0을 주도한다. 위상 2(보라색)는 120도까지 위상 0을 추적하고 있다. (이 수치에서 $x = 25$ 일 때, 각도는 π 라디언)

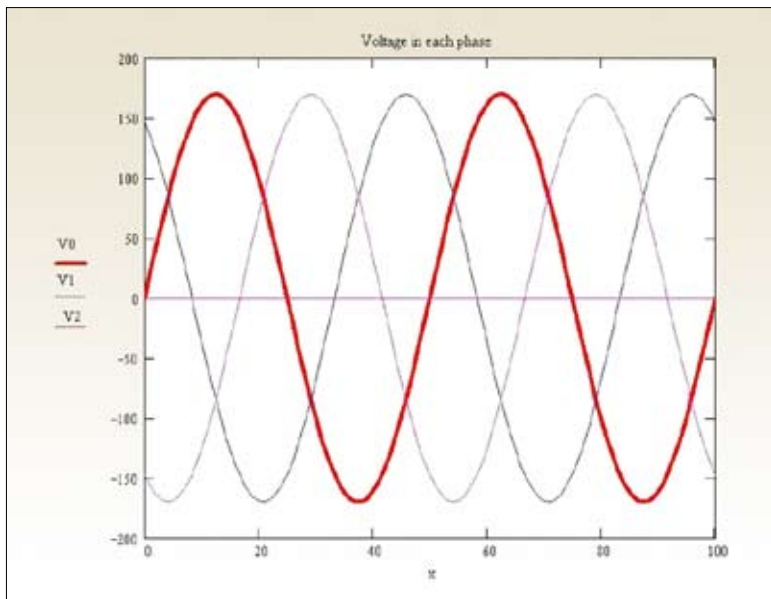


그림 1: 시간의 함수로써 전압을 보여주는 3상 전력 라인의 전압 파형

처음 이 문제가 나타날 때, 대부분의 설계자는 프론트 엔드 상의 PFC 컨버터에서 구동하는 3상 정류기가 솔루션을 제공한다고 가정할 것이다.

설계자가 3상을 채택해 그림 2처럼 PFC에 3상을 연결한다면, 3가지의 리드에서 전류 파형은 올바른 결과가 나오지 않을 것이다.

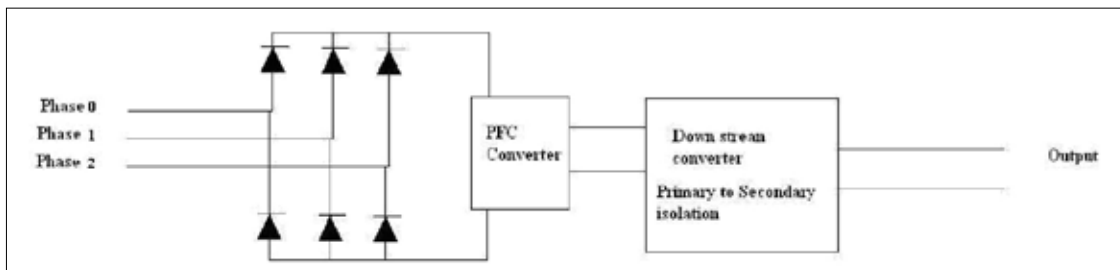


그림 2: 실행 불가능한 3상 PFC

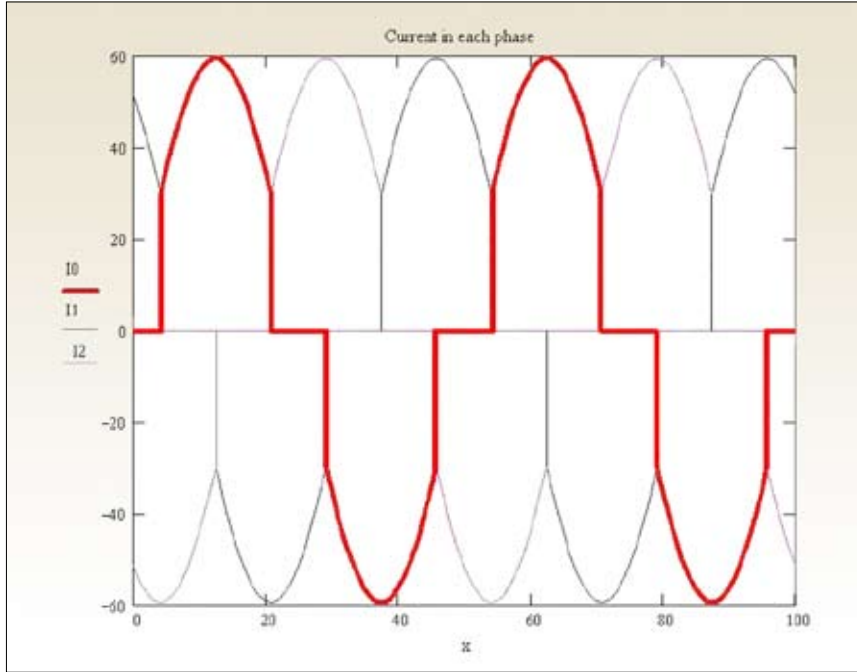


그림 3: 그림 2의 회로 결과에 따른 전류

그림 3의 파형에서처럼, 각 위상에서 전류는 실제 전압이 제로 볼트 이상이라고 하더라도, 상당부분 시간이 불연속적이다. PFC 회로는 PFC에 대한 입력 전류가 라인과 중립 사이에 연결된 레지스터가 진행되는 것처럼 보이게 하는 것이 중요하다. 따라서, 전류 파형은 전력 소비를 가능하게 하는 스케일링을 이용해 그림 1의 전압처럼 동일하게 해야 한다.

여기에 필요한 솔루션은 각 라인을 위한 PFC 함수를 제공하는 것으로, 동시에 각 라인의 부하가 균형되어야 한다. 이는 3가지의 메인 빌딩 블록과 함께 부속 회로를 필요로 한다.

각 라인의 첫 번째 회로에서는 시스템으로 들어오는 것이 PFC 컨버터 섹션이라는 것을 볼 수 있으며, 이것은 각각에서 독립된 3가지 PFC 컨버터로 구성되어 있다. 이러한 설계는 약 50% 이상의 전력을 순간적으로 허용해야 하지만, 약 15% 정도의 더 많은 전력이 온도상으로 허용되어야 한다. PFC 섹션의 설계는 참조 1에 기술되어 있다.

두 번째 시스템 단계는 다운스트림 컨버터이다. 이 컨버터 제품들은 부하를 구동시키기 위한 출력의 위치이다. 절연은 각 컨버터의 입력 출력 사이에 필요하며, 모든 출력은 서로 연결될 것이다. 모든 장치들은 작동해야 하며, 함께 움직여야 한다. 따라서, 이러한 장치용 컨트롤러는 컨버터의 2차 측에 위치되어야 한다.

각각의 다운스트림 컨버터는 공통의 접지 포인트에서 독립형 장치로써 동작해야 한다. 그러나, 이 컨버터 제품 모두는 서로 연결되어 부하를 공유할 수 있다. 2차 컨버터가 독립적으로 동작해야 하는 이유는 각 장치의 입력 전압이 서로 다른 PFC의 출력이기 때문으로, 이들은 서로 다른 입력 레벨이다. 이것은 개별적인 컨트롤러를 요구한다. 이 때, PFC 컨버터 출력 각각은 2배의 라인 주파수에서 중요한 리플과 120도 위상 차이를 가지고 있다.

또한 이 지점은 출력이 부하를 공유해야 하는 곳이기 때문에, 단일 컨트롤러는 동작하지 않을 것이다. 컨트롤러가 전류 레벨이 부하 공유가 되도록 조정해야 하기 때문이다. 따라서 이러한 컨버터 설계는 리모트 센싱을 통합해야 하며 부하를 공유할 수 있도록 해야 한다.

3상 입력을 사용한 전력 레벨에서, 위상 변경 풀 브리지는 서로 다른 토폴로지에서 여러 장점을 제공한다. 위상 변경의 풀 브리지 컨버터의 1차 측에서 전력 스위치들은 트랜스포머를 통해 구동된다. 모든 3상 변경 컨트롤러는 동일한 부하를 구동시키기 위해 필요한데, 이것은 어디에서 절연이 제공되는가에 대한 단계이기 때문에 2차 측에서 제어 IC를 갖추는 것이 합리적이다. 트랜스포머의 사용을 통해, 이와 같은 경우에 필요한 절연 기능이 제공된다.

3단계는 부하 공유 회로이다. 이 단계는 각각의 다운스트림 컨버터에서 출력을 모니터링하며, 출력들이 부하를 동일하게 공유할 수 있게 한다. 이것은 차례로 PFC 섹션을 동일한 전력 양을 입력 라인으로 끌어올 수 있게 하며, 그 결과 3상에서 부하 밸런싱의 효과를 거둘 수 있다.

그림 4는 3상 역률 보정을 달성하기 위해 필요한 기본적인 회로이다.

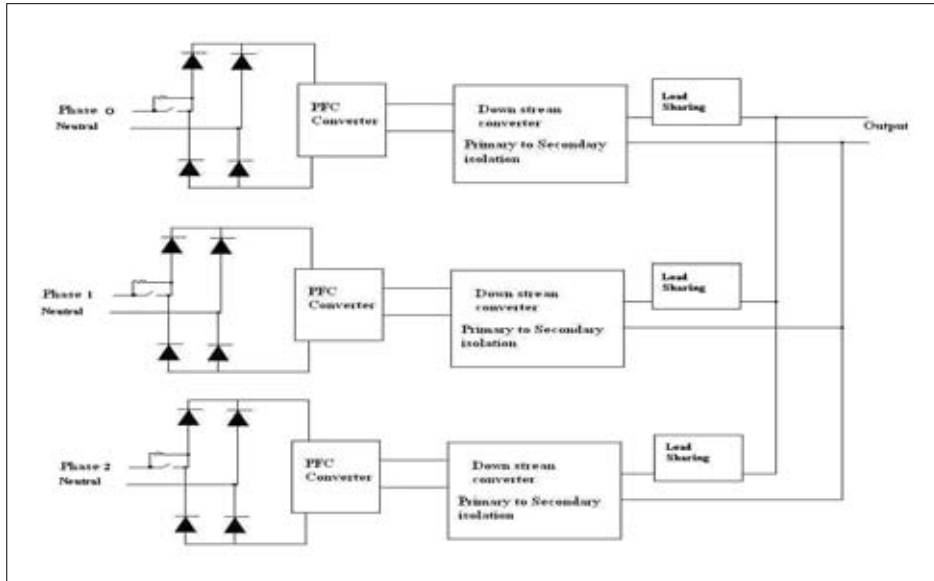


그림 4: 입력 전류 제한 제어를 포함한 기본적인 3상 PFC 회로

보조 회로는 하우스키핑 전력, 동기화, 스타트업, 모니터링 등 다른 기능을 위해 제공한다.

보조 회로의 첫 번째는 내부 보조 전원 공급장치이다. 모든 PFC 컨버터는 절연된 공급장치에서 전원을 공급 받아야 하며, 2차적인 컨트롤러 및 다른 여러 보조 회로는 2차 컨버터가 전력을 공급 받기 전에 절연된 전력을 요구한다. 개별적인 하우스키핑 컨버터는 필수적인 기능이다. PFC 섹션의 각각은 동일하기 때문에, 이 하우스키핑 컨버터는 1차 측의 PFC 컨버터 각각에 절연 출력으로 자체 3상 정류를 갖추며, 2차 측 다운스트림 컨버터와 전류 공유 회로에 대한 출력을 갖는다.

또 다른 필수적인 회로는 스위치/전류 제한의 형태로, 대규모 전류 펄스나 PFC 출력 전압의 공진형 오버슈트 없이 PFC 출력 커패시터의 초기 충전을 가능하게 한다. 이것은 릴레이 및 레지스터로써, 그림 4에 제시되어 있다. 릴레이가 활성화되어 PFC가 동작을 시작하기 전에, 레지스터는 PFC 커패시터의 출력을 충전할 수 있다. 이것은 각 PFC의 출력 커패시터 전압 및 릴레이 드라이버의 절연형 전압 모니터링을 요구한다. 이 때, 보조 전원은 릴레이에 전압을 주는 전력을 제공하며, 전력은 이 섹션을 최대 전력을 가져올 수 있는 PFC 섹션을 제공한다.

일단, 3가지의 모든 PFC가 구현되고 최대 전압으로 실현되면(이는 2차적인 전압 모니터링을 필요로 한다), 모든 2차 컨버터는 동시다발적으로 전력을 공급 받게 된다. 또 소프트스타트 하에서 실현될 수 있어 동일한 속도에 이를 수 있다. 모든 컨버터들이 출력에서 동일한 접지 포인트를 갖기 때문에, 동시 동작형의 스타트를 달성하는 회로는 상대적으로 설계하기 쉽다. 모든 PFC 출력이 최대 값을 갖기 위해, 각각의 PFC에서의 모니터 회로는 PFC 출력 전압을 모니터링하고, 옵토커플러를 구동시키는 1차 측에서 비교기만큼 단순해진다. 옵토커플러의 광 트랜지스터가 직렬로 연결되고 세 가지 모두 활성화될 경우, 이것은 전압을 하강시키고 3개의 컨버터를 해방시킬 것이다.

각각의 다운스트림 컨버터들은 컨버터의 출력 전압 레벨 세트에 도달한다. 때문에 이 컨버터들이 자신들의 전류를 단계적으로 되돌려 주고, 과전압 셋다운으로 진행되지 않게 하는 것이 중요하다. 이는 또 다른 컨버터들이 출력 전압을 지속적으로 상승시킬 때, 출력 전압이 일정 수준까지 상승하기 때문이다. 각기 최대 전류에 도달될 때, 최대 전류로 진행되어야 하며 셋다운 되어서도 안 된다. 이것은 전류 공유 회로 시간이 동작할 수 있고, 부하를 공유해야 하기 때문에 필수적이라고 할 수 있다.

물론, 극도의 과전압은 모든 장치들은 셋다운 시켜야 한다. 전류가 너무 과도할 경우에 장치는 전류를 제한해야 하며, 출력 단락의 경우에는 손상을 막기 위해 단락 지연 이후 셋다운 되어야 한다.

또 다른 회로는 모든 컨버터가 동일한 주파수로 동기화되기 위해 필수적이다. 보통, PFC/다운스트림 컨버터 구성에서, PFC는 다운스트림 컨버터로 동기화된다. 그러나 3가지의 다운스트림 컨버터가 존재하기 때문에, 하나는 마스터가 되어야 하며 또 다른 것들은 슬레이브가 되어야 할 것이다. 각각의 PFC/다운스트림 컨버터 결합은 동일해야 것이 바람직스럽기 때문에, 모든 것이 내부 하우스키핑 컨버터로 동기화되거나 일부 복합적인 컨버터로 동기화할 것을 추천한다.

Three-Phase Power Factor Correction Circuits for Low-Cost Distributed Power Systems

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Three-Phase Power Factor Correction Circuits for Low-Cost Distributed Power Systems

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Electrical and Computer Engineering

(Abstract)

Front-end converters with power factor correction (PFC) capability are widely used in distributed power systems (DPSs). Most of the front-end converters are implemented using a two-stage approach, which consists of a PFC stage followed by a DC/DC converter. The purpose of the front-end converter is to regulate the DC output voltage, supply all the load converters connected to the distributed bus, guarantee current sharing, and charge a bank of batteries to provide backup energy when the power grid breaks down.

One of the main concerns of the power supply industry is to obtain a front-end converter with a low-cost PFC stage, while still complying with required harmonic standards, especially for high-power three-phase applications. Having this statement in mind, the main objective of this dissertation is to study front-end converters for DPS applications with PFC to meet harmonic standards, while still maintaining low cost and performance indices.

To realize the many aforementioned objectives, this dissertation is divided into two main parts: (1) two-stage front-end converters suitable for telecom applications, and (2) single-stage low-cost AC/DC converters suitable for mainframe computers and server applications. The use of discontinuous conduction mode (DCM) boost rectifiers is extensively explored to achieve simplicity, while reducing the cost for DPS applications. Interleaving of DCM boost rectifiers is also explored as an alternative approach to further reduce the system cost by reducing the filtering requirements. All the solutions discussed are implemented for 3kW applications, while 6kW is obtained by interleaving two converters

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“Lezinha, você é muito especial”

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List of Acronyms

AC: alternating current
CC: Cauer-Chebyshev
CCM: continuous conduction mode
CM: common mode
DC: direct current
DCM: discontinuous conduction mode
DM: differential mode
DPS: distributed power system
EMI: electromagnetic interference
IEC: International Electrotechnical Committee
LISN: line impedance stabilization network
LN: line-to-neutral
NPC: neutral-point-clamped
PFC: power factor correction
PWM: pulse width modulation
RMS: root mean square
THD: total harmonic distortion
TL-AS: three-level asymmetrical
TL-PS: three-level phase-shift
ZCT: zero-current transition
ZVS: zero-voltage switching
ZVZCS: zero-voltage and zero-current switching

1. Converters for Distributed Power Systems

A distributed power system (DPS) offers many advantages from the standpoint of high power capability, reliability, modularity, redundancy and maintainability [1]. As a result, DPS has become rather popular in telecom and server applications. For centralized power supplies, the reliability must be very high, since a failure would cause the entire system to shut down. However, the failure of any power module in a DPS has a reduced effect on the overall system because of the built-in N+1 redundancy, where N is the minimum number of modules needed to supply the load. Additional advantages of DPS are rapid replacement of faulty modules and flexibility to expand the system capacity as the load requirements increase [2].

Despite several important advantages, a DPS offers two major drawbacks: (1) extra cost and (2) noise caused by several converters placed next to each other [3]. Thermal issues may arise because the power supplies are either compressed into ever-smaller cases or because they are mounted on the logic boards to which they supply power. Nevertheless, paralleling decreases the dissipation per module because each module is required to handle less power in the system, which helps simplify thermal design [1].

A typical block diagram of a DPS is illustrated in Fig. 1-1. As can be seen, a DPS consists of several stages of power conversion. The name distributed power systems alludes to the fact that the power processing units in the system may not be located in the same place, but are distributed according to load type and location [1] [2]. For the structure shown in Fig. 1-1, the front-end converter is supplied by an AC power source, which can be either a single- or a three-phase bus. The power is processed by the DPS front-end converters represented by the power supplies (PSs)

#1 through #N+1 in Fig. 1-1. Each PS consists of a power factor correction (PFC) stage and a DC/DC front-end converter used to regulate the 48V DC distributed power bus. Small DC/DC high-density power modules are then distributed according to load requirements and location to provide point-of-load regulation. Besides supplying power to the load, the front-end converter for telecom applications, for instance, is also used to charge the backup batteries connected across the distributed DC bus voltage (not shown in Fig. 1-1). As described in section 1.4, the work described hereafter concentrates on the front-end converter of the DPS. The load converters are not discussed in this dissertation, as they have already been approached by other authors [4] [5].

Front-end converters for DPS applications are typically used in telecom and server applications. There is a wide range of front-end converters available in the market for telecom applications, with power levels ranging from hundreds of watts to several kilowatts. For server applications, the typical power level is 1kW. However, the market for sever applications is growing quickly, as is the power level required for such applications. As predicted in the past, computer applications will continue to drive the power supply industry and to promote the widespread use of DPSs [3].

The PFC stage of the front-end converter has become an important accessory because, especially in Europe, several standards are now limiting the emission of harmonic currents caused by electronic equipment [6]-[8]. However, it has always been difficult to justify the cost incurred by adding the PFC stage to the DPS front-end converters, especially for high-power applications (6kW and up). Consequently, the research on PFC circuits for high-power applications is still open in terms of finding solutions able to significantly reduce cost. Obviously, the performance

of the DPS front-end converter must be preserved, despite any cost reduction in the front-end PFC circuit. Reducing the cost of the PFC stage, while preserving the overall performance indices of the DPS front-end converter is rather challenging. As a result, this issue needs to be carefully addressed.

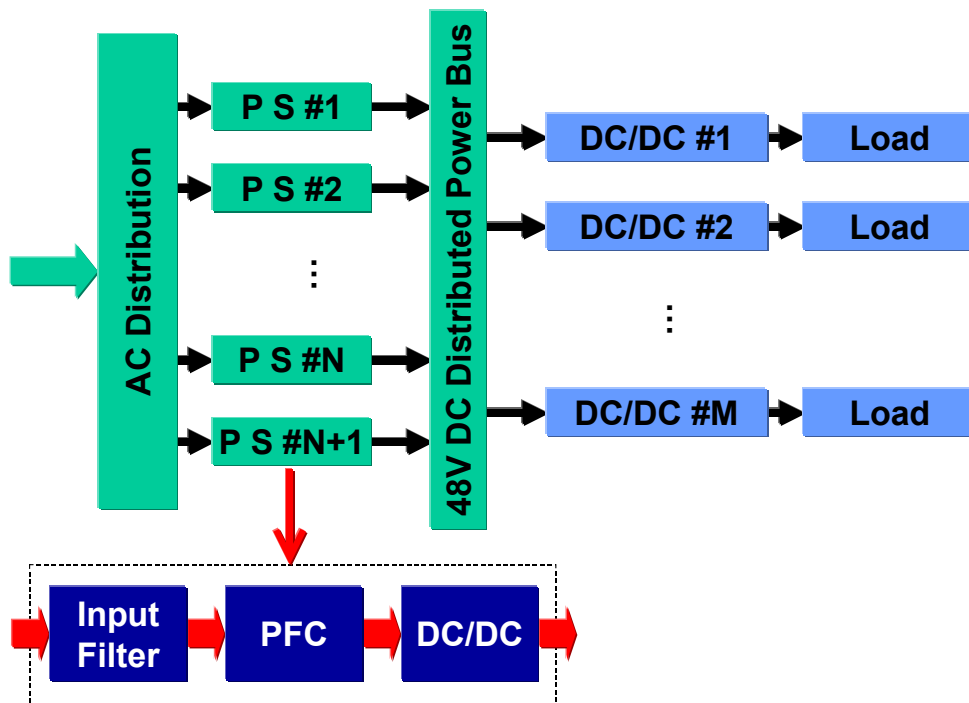


Fig. 1-1. Distributed power system configuration.

1.1. High-Power State-of-the-Art DPS Front-End Converters

For the next generation of high-power DPS front-end converters, not only the overall performance but also the cost of the entire system will be important issues to be considered during the design process. The front-end converter for DPS applications must achieve high power factor, low harmonic distortion, high efficiency, high power density, high reliability and low electromagnetic interference (EMI) noise. To reduce the cost of the front-end converter, the PFC stage must be inexpensive, while still complying with standards for harmonic distortion.

One of the conventional practices, commonly used to obtain high-power DPS front-end converters, is the use of a two-stage approach based upon single-phase power modules, as discussed in previous papers [9]-[11] and shown in Fig. 1-2. That figure shows that the first stage of each module is used to perform the PFC function to meet harmonic current standards such as the IEC 61000-3-2, while the second-stage DC/DC converter regulates the DC output voltage of the system and guarantees system current sharing.

The PFC circuit of each module operates in the continuous conduction mode (CCM) and is controlled by average current mode control. The performance of the two-stage approach is high, but so is the cost involved because of the number of components used to realize the system. Moreover, to operate in CCM, the single-phase PFC circuit requires a complex control, as well as a large intermediate bus capacitor to limit the bus voltage ripple and handle the pulsating power in the intermediate DC-link bus. Nevertheless, the two-stage DPS using single-phase front-end modules has the advantage of modularity, which is also a measure of performance, while N+1 redundancy is also easily achieved.

A possible approach for reducing the cost of the front-end converter is to simplify the PFC stage. Connecting the three outputs of the single-phase boost rectifiers eliminates the pulsating power in the high-voltage DC-link intermediate bus, while permitting the use of only one DC/DC converter, as shown in Fig. 1-3. In this way, the volume of the intermediate bus capacitor can be reduced [12] because the pulsating power is eliminated. However, the direct connection of the outputs of the single-phase boost rectifiers creates interactions between the PFC circuits.

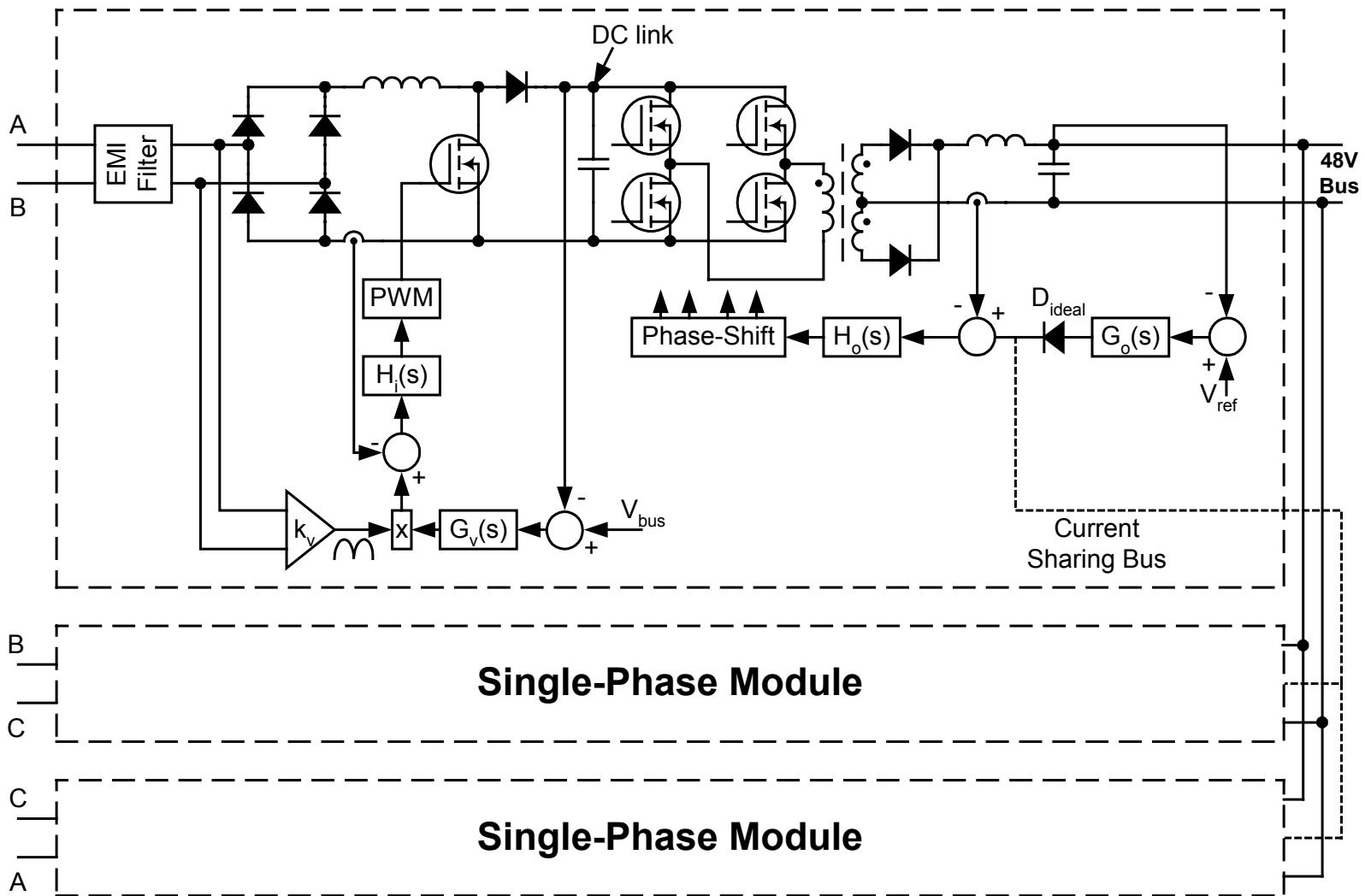


Fig. 1-2. High-power DPS front-end converter using three single-phase modules.

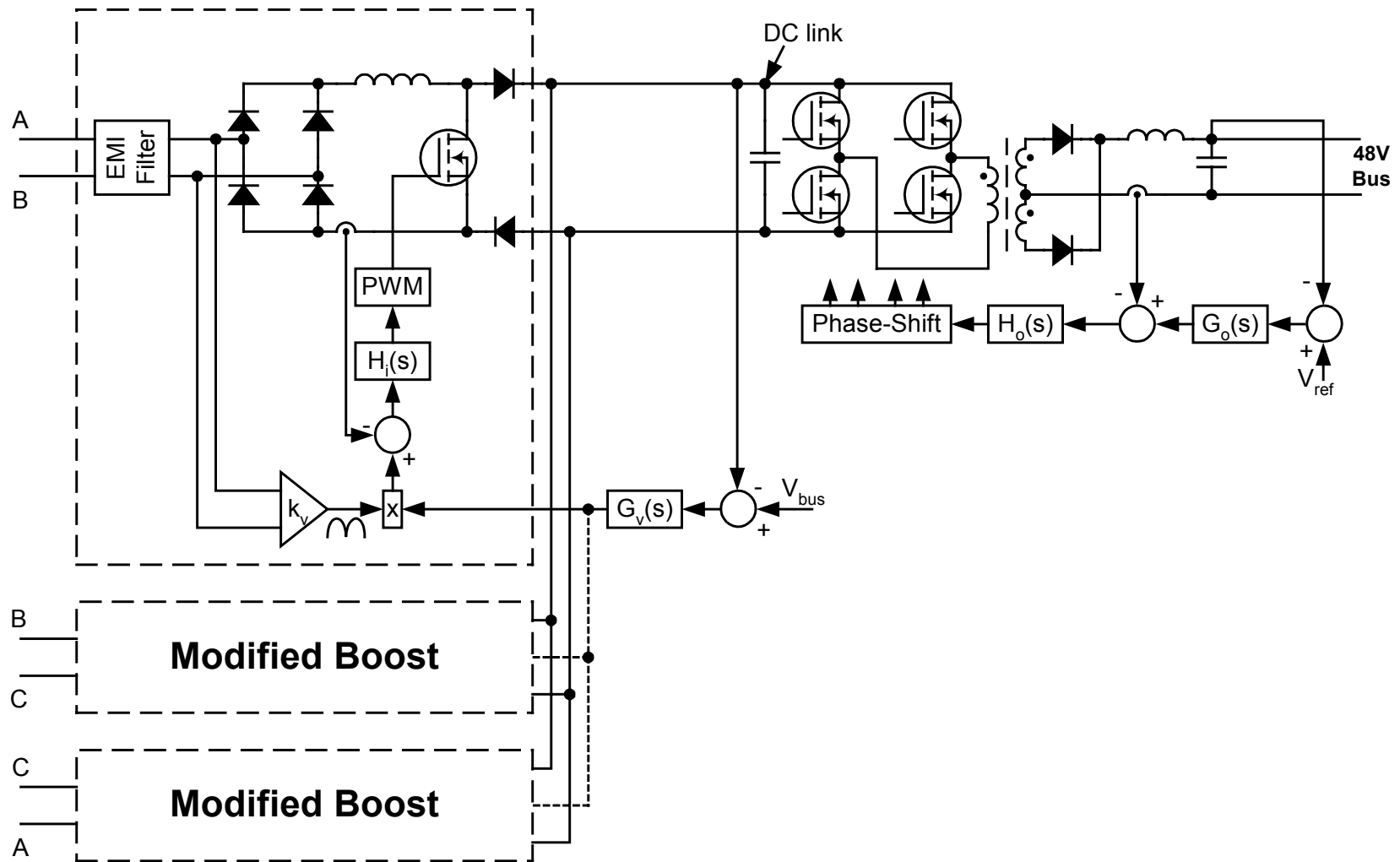


Fig. 1-3. Simplified front-end converter using three single-phase rectifiers connected to the same output.

To mitigate the interactions in the structure shown in Fig. 1-3, the boost inductor is split into two parts, while a diode is added to the circuit configuration of each single-phase boost rectifier. For proper operation, the intermediate bus voltage must be at least twice the peak input voltage, which means that the voltage rating of the boost power switches must be at least 800V in applications for which the nominal line-to-line input voltage is 380V. Eventually, the switches of the DC/DC converter will experience higher voltages stress unless a three-level structure is used for the DC/DC converter [13]-[16]. Another approach used to reduce the cost of the DPS has been reported [17]. However, that system has been implemented for 500W of total power, and a three-phase line-to-line voltage of 200V has been selected in order to limit the voltage stress across the Sepic switch to less than 500V. For higher-input-voltage applications, the Sepic converter requires switches with much higher voltage rating, which makes the solution not viable for most applications.

A significant breakthrough in simplifying the single-phase modules was achieved by some rectifiers [18] [19], as shown in Fig. 1-4(a). The VIENNA rectifier can be seen as a simplified version of three single-phase PFCs connected to the same intermediate bus voltage, as illustrated in Fig. 1-3. The main idea behind this simplification is to use the neutral-point connection of the split bus capacitors to reduce the voltage applied across the power switches. For proper operation, the bus voltage still needs to be at least twice the line-to-neutral peak input voltage. However, the three-level structure obtained by using the neutral-point connection reduces the voltage stress across the switches to half of the total bus voltage, thus allowing 500V MOSFETs to be used in the VIENNA rectifier. Another version of the VIENNA rectifier was presented

[20]. However, that version of the VIENNA rectifier did not split the bus capacitors, and for this reason it could not solve the problem of the voltage stress across the power switches.

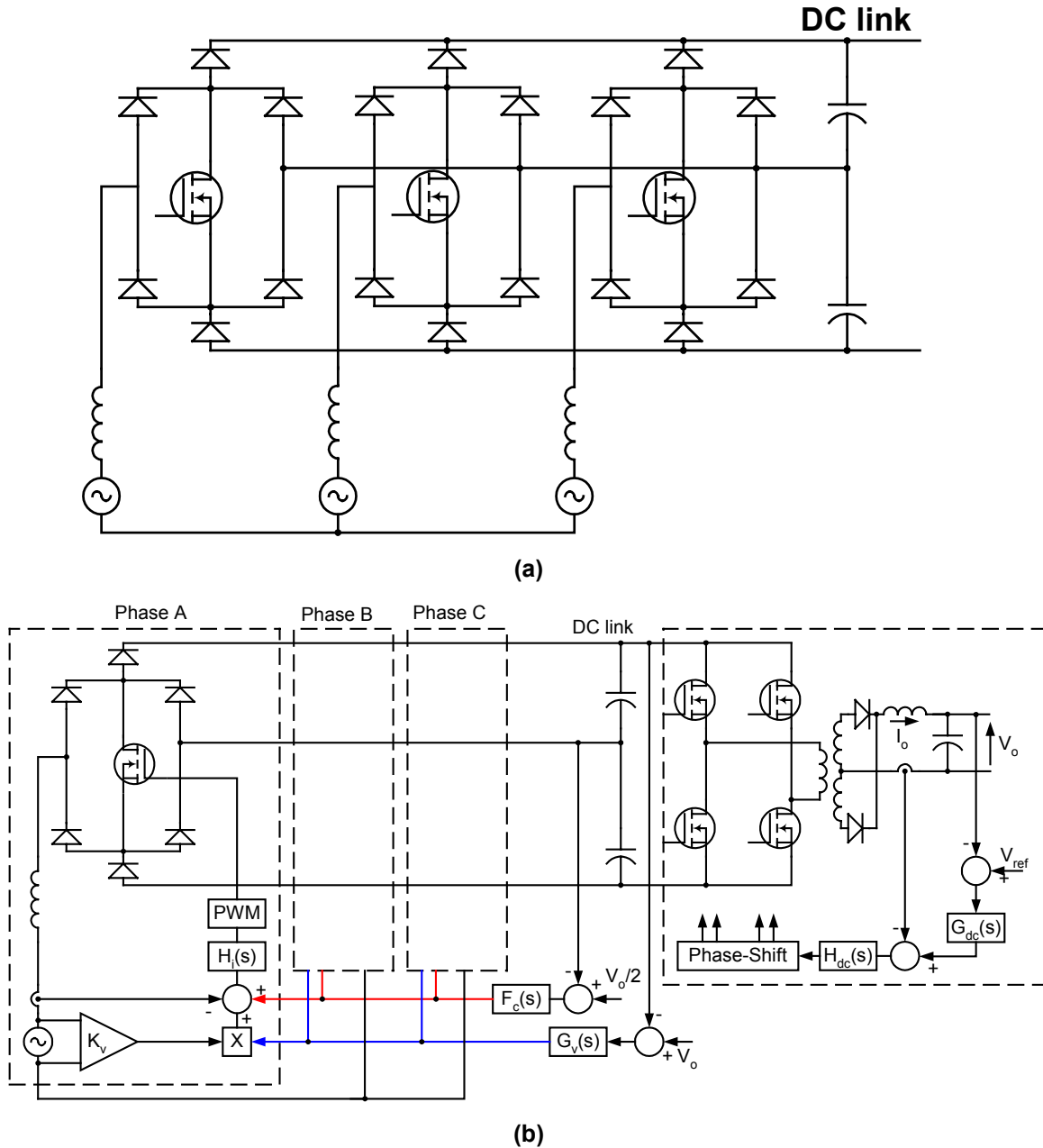


Fig. 1-4. Using the VIENNA rectifier in the PFC stage of the high-power front-end converter: (a) VIENNA rectifier and (b) control block diagram and connection of DC/DC converter.

In the VIENNA rectifier, the switches of the DC/DC converter must resist the total bus voltage, as illustrated in Fig. 1-4(b). There are two possible ways to overcome this problem: the

individual DC/DC converters can be connected across each bus capacitor, or a three-level DC/DC converter can be used to reduce the voltage stress across the power switches [21]. Another important achievement of the VIENNA rectifier is that a phase-leg integrated power module can be purchased to implement each leg. The integrated module is provided by IXYS as part numbers VUM 25-05 and VUM 85-05. Both modules consist of the integration of the power switch, the diodes of the single-phase bridge, and the two fast diodes (one connected to the positive and the other to the negative intermediate DC bus rail).

1.2. General Approaches to Three-Phase PWM Rectifiers for High-Power Applications

1.2.1. Rectifiers With Bi-Directional Power Flow Capability

There are many other approaches that can be used to enhance power quality in high-power applications. Among the three-phase rectifiers, the six-switch boost topology is able to achieve the best performance in terms of shaping the input currents and presenting reverse energy flow capability [22] [23] [24]. However, as shown in Fig. 1-5(a), it is necessary to use IGBTs instead of MOSFETs because of the high bus voltage processed by the boost-type rectifier. High-voltage MOSFETs add conduction loss to the circuit, thus reducing the efficiency. Additionally, when MOSFETs are used in the circuit, the anti-parallel diodes will present serious reverse-recovery problems due to the high operating frequency. To improve the efficiency of the six-switch boost rectifiers, several soft-switching schemes and lossless snubbers have been presented [24] [25] [26]. Either soft-switching circuits or lossless snubbers add cost to the system, making these solutions difficult for industry to accept. Further improvements in switching and conduction losses have also been achieved by applying special modulation schemes that optimize the

conduction of the power switches within the line period [27]. Although MOSFETs are not the best device choice for six-switch boost rectifier applications, one has to be cautious when using IGBTs because their turn-off loss limit the switching frequency to well below 40kHz, except if soft-switching schemes are used to improve the turn-off conditions for the IGBTs.

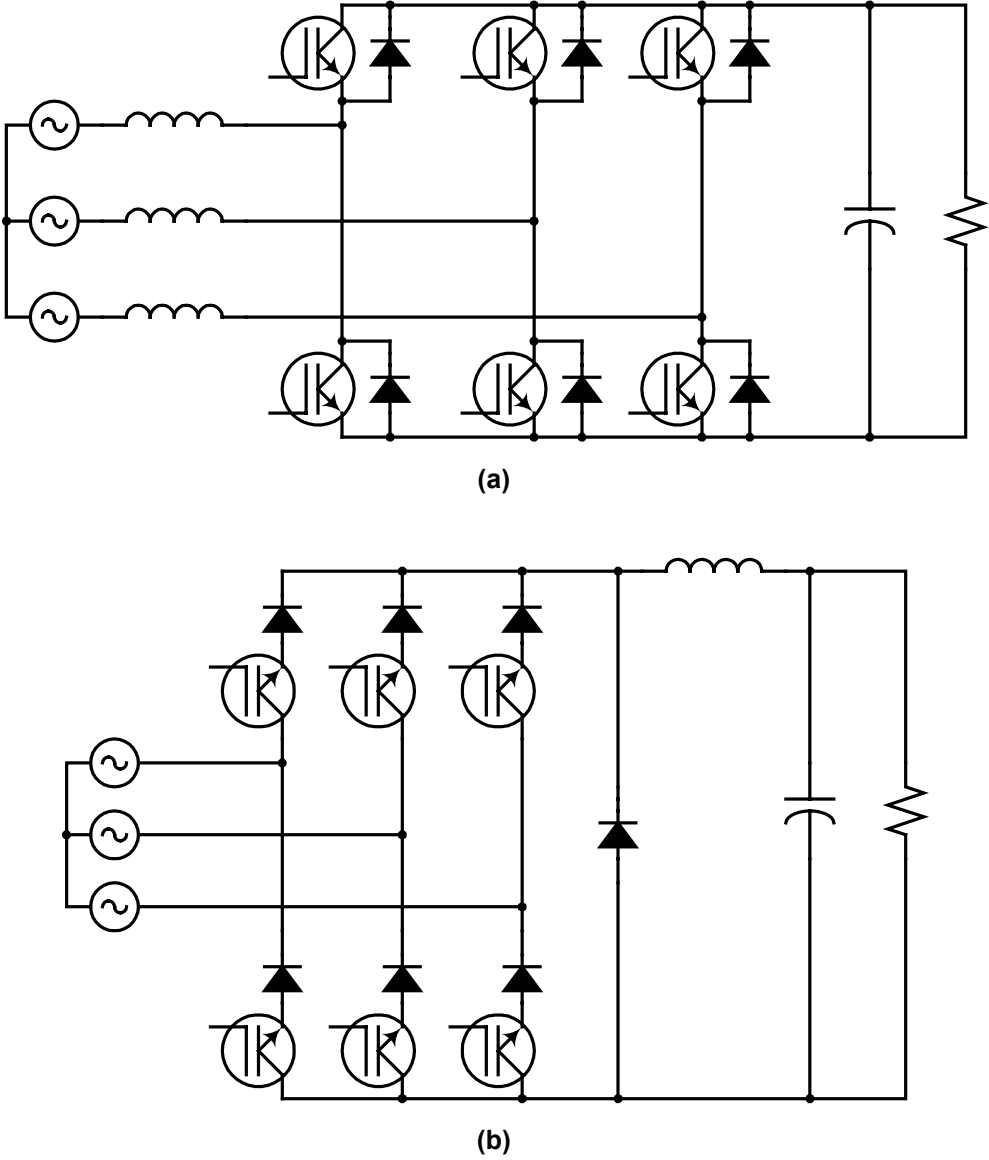


Fig. 1-5. Three-phase rectifiers: (a) boost and (b) buck.

Buck-derived rectifiers can also draw sinusoidal input currents from the mains [28] [29] [30] [31] [32] [33]. The buck rectifier offers some advantages over the six-switch boost approach,

such as the step-down voltage capability, short-circuit protection, inherent control of the inrush current, and low bus capacitance. On the other hand, the major disadvantages of the buck rectifiers, as compared to the boost topologies, are the pulsating input currents and the conduction loss caused by several voltage drops in the path of the inductor current. As shown in Fig. 1-5(b), a freewheeling diode can be used to reduce the conduction loss in the buck rectifier. However, this solution eliminates rectifier's ability to handle bi-directional power flow.

1.2.2. Rectifiers With Unidirectional Power Flow Capability

The unidirectional PFC approach is a good option for reducing the cost of the front-end PFC stage [18] [19]. Examples of unidirectional PFC approaches have been proposed [34] - [36], as depicted in Fig. 1-6(a). The circuit under consideration is able to provide PFC over a wide input voltage range. At high-line input voltage, the range switch must be open, while the range switch must be closed at low-line input voltage in order to increase the rectifier voltage gain. The circuit shown in Fig. 1-6(a) uses the upper switch to control the most positive input current and the lower switch to control the most negative input current. Since the rectifier is able to control only two input currents at a time, selecting one of the three low-frequency switches according to the input voltages actually indirectly controls the third line current as well. The three low-frequency switches can be easily realized by one of the configurations shown in Fig. 1-6(b). The low-frequency switches do not experience switching stresses, and the RMS current is reduced because of the short conduction interval within the line cycle.

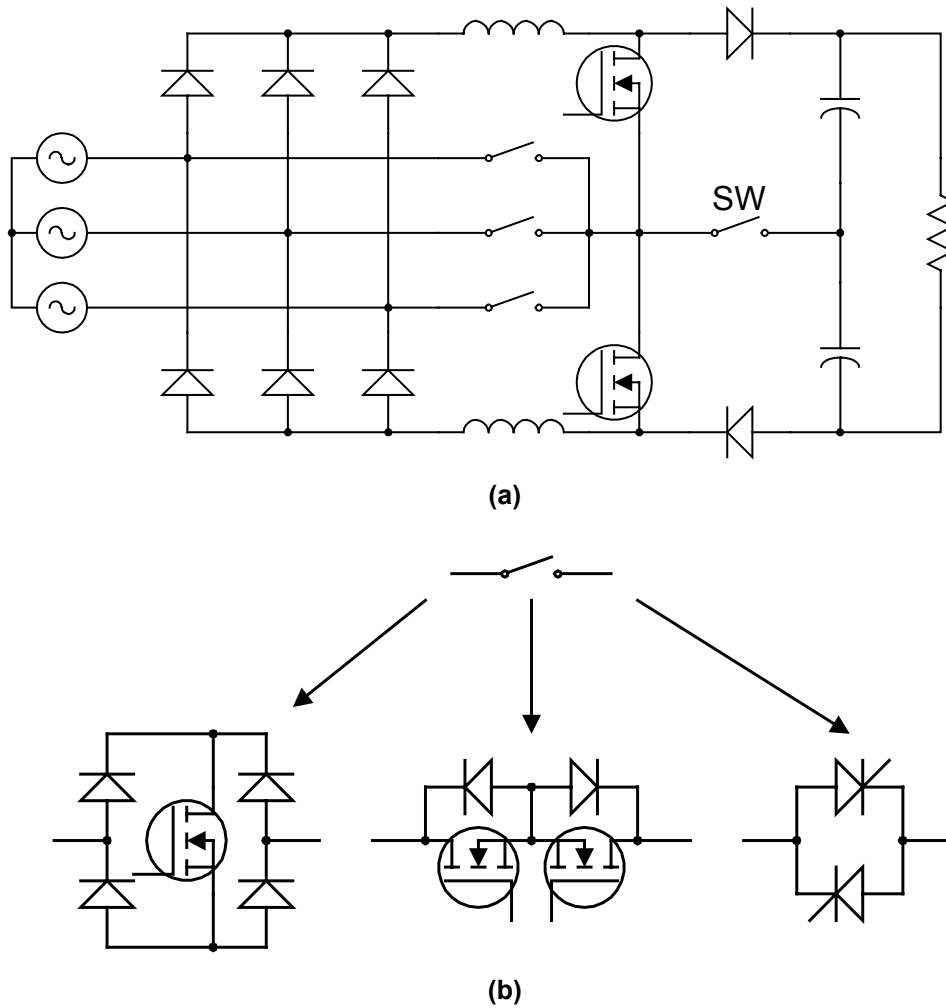


Fig. 1-6. Unidirectional PFC used for wide input voltage range: (a) topology with range switch and (b) different ways of realizing the three low-frequency switches.

1.2.3. Low-Frequency Rectifiers

For very high-power applications, low-frequency PFC topologies have been used as low-cost front-end PFC circuits. The use of low-frequency rectifiers, however, implies that size is not a requirement. One example of a low-frequency rectifier is the three-phase, three-level boost topology shown in Fig. 1-7(a). For this application, the three-level rectifier operates at low frequency, and the power switches shape the input currents by conducting during short intervals

within the line period. Although the total harmonic distortion (THD) of the input current is relatively low at heavy load, it drastically increases as the output power decreases [37].

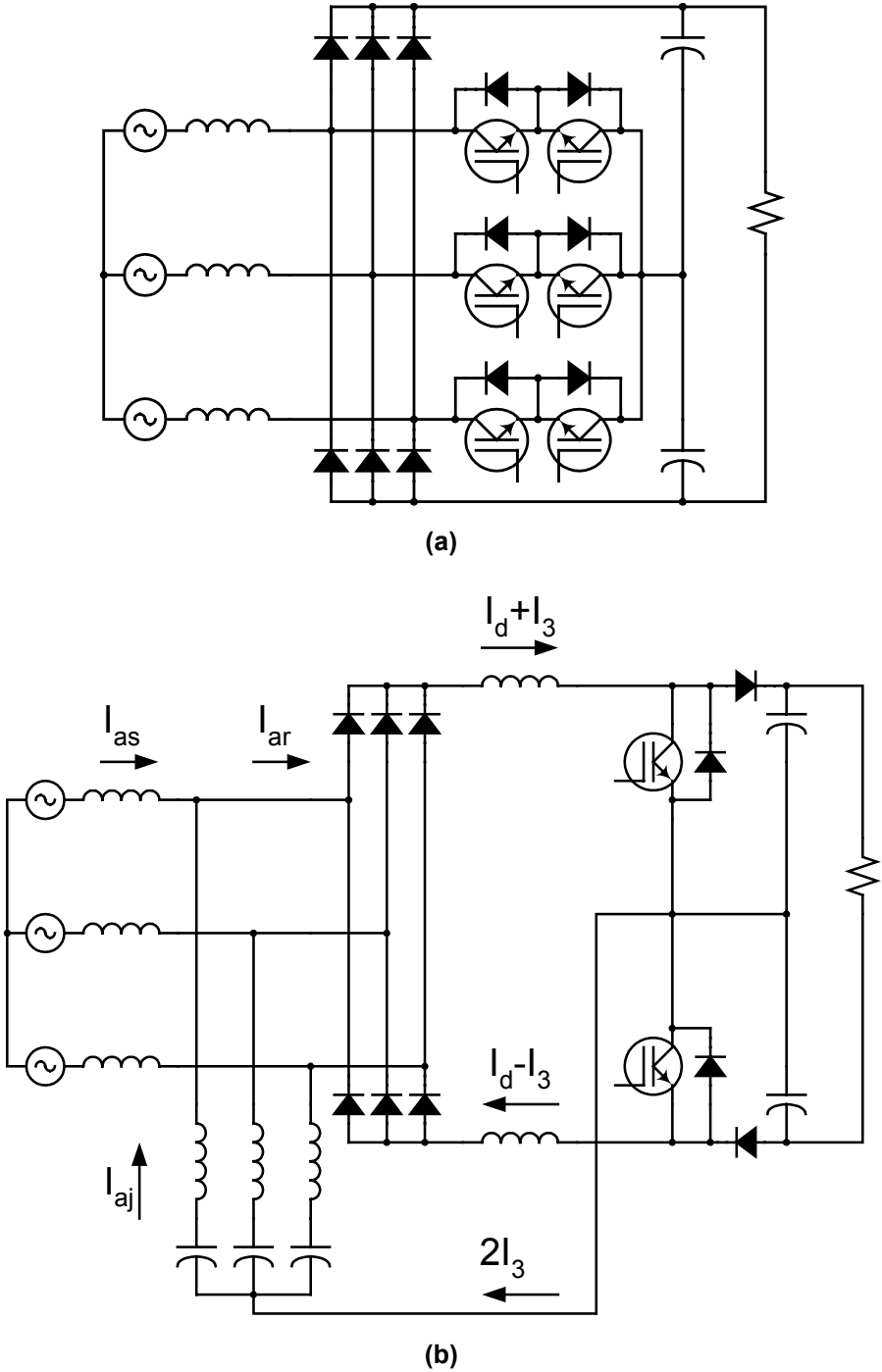


Fig. 1-7. Low-frequency PFC solutions: (a) three-level PFC topology and (b) injecting third harmonic.

The third-harmonic injection method is also an option for high-power PFC applications [38] [39], as illustrated in Fig. 1-7(b). The switches are operated at high frequency in order to control the currents through the DC-side inductors. However, despite the high-frequency operation of the power switches, the series network must be tuned around the third harmonic of the line frequency to provide low THD for the input current. As a result, the size of the converter is large because of the low series resonant frequency.

1.2.4. Active Filters

Another option for very high-power installations is the use of either a shunt or a series active filter, or a combination of both, to improve the quality of the input currents generated by non-linear loads [40] [41], such as power supplies. This type of solution is centralized and does not require local PFC capability for individual loads. Fig. 1-8(a) illustrates a shunt active filter used to shape the input source current. The active shunt filter is not connected to the main path of the input current. Therefore, the active shunt filter is required to process only part of the total load power, as opposed to rectifiers that are always required to process 100% of the power. Two simulation results are provided in Fig. 1-8 to demonstrate the extent to which the use of active shunt filters is advantageous when compared to rectifiers. For both simulation results, the load requires a total active power of 15kW. In Fig. 1-8(b), the current THD generated by the load is 30%, which requires the active filter to process only 3.6kVA. On the other hand, Fig. 1-8(c), shows that the higher load current THD requires the active filter to process much more apparent power. For this example, the active filter has to process 16.2kVA, which is even higher than the active power required by the load. Therefore, these two simulation results show that the use of active shunt filters is advantageous when the harmonic distortion generated by the load is not too

high. If that is not the case, rectifiers are still the preferred solution for enhancing the quality of the source AC current.

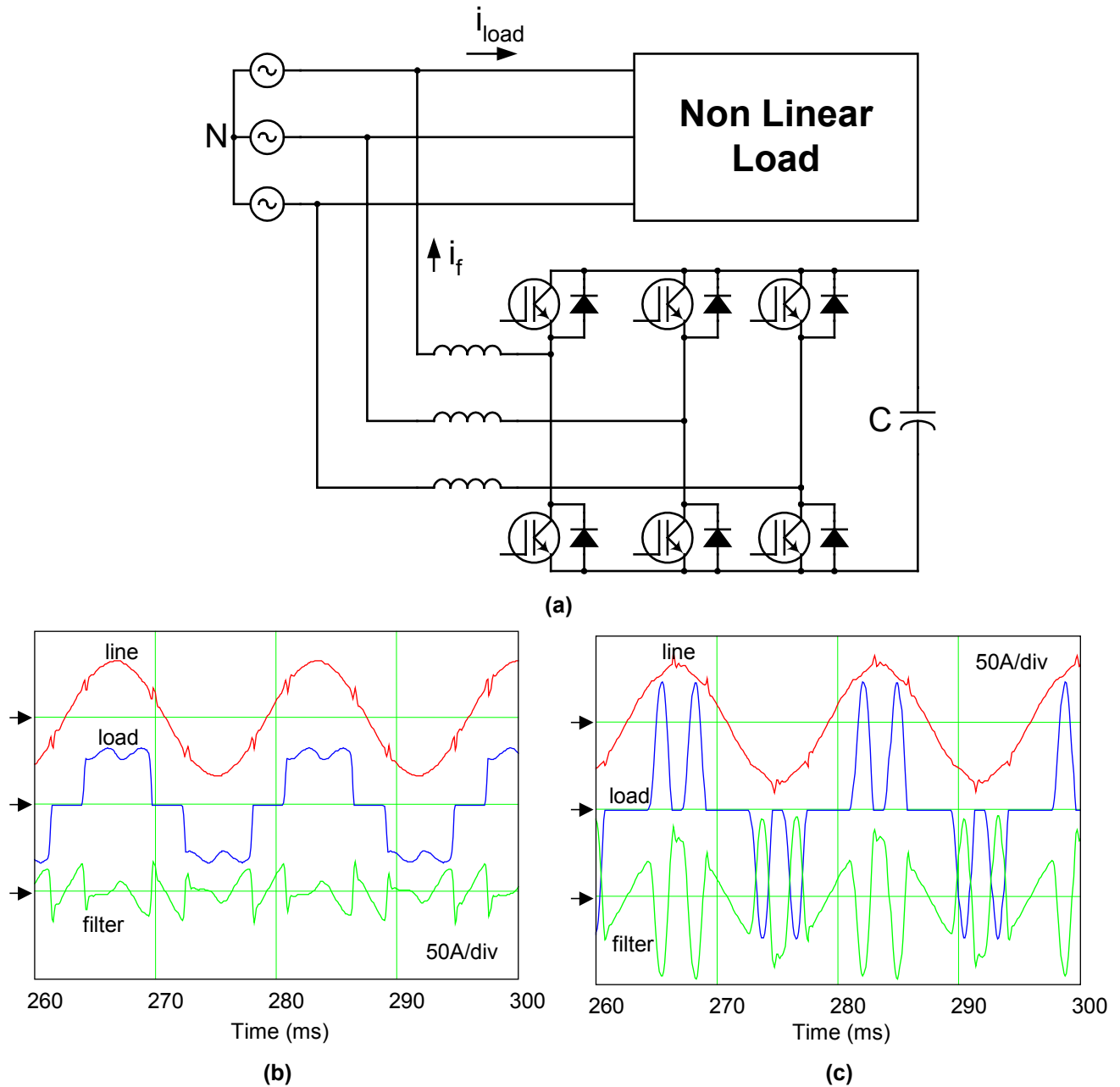


Fig. 1-8. Active shunt filter used to improve the current waveform generated by non-linear loads: (a) structure, (b) 30% of THD produced by the load current, and (c) 100% of load current THD.

1.3. Defining the Benchmark Circuits for Comparison (Baseline)

Because several comparisons will be made during the course of this dissertation, it is rather important to have a baseline with which compare the results that will be presented hereafter. A benchmark circuit should be based on some kind of practice widely adopted in industry. For the PFC front-end stage, the state-of-the-art approaches for high-power DPS applications are based upon the three single-phase modules and the VIENNA rectifier. Therefore, throughout the course of this dissertation, the results that are obtained will be compared against the benchmark circuits shown in Fig. 1-2 and Fig. 1-4. Several aspects are benchmarked, including size of the differential mode (DM) input filter, size of the boost inductors, and device stress.

1.4. Dissertation Outline

The front-end converters for DPS applications are extensively used in telecommunication systems to supply load converters and to charge batteries to provide backup energy during power grid blackouts. Besides telecom front-end converters, mainframe computers and server applications also require front-end converters to distribute power to the loads. Although the typical power level for server applications is 1kW, it is envisioned that in the future high-end servers will demand more power, which justifies the development of front-end converters for high-end server applications as well.

There are two major reasons for developing research on PFC circuits used for high-power DPS applications. The first reason is to improve power quality, since the harmonic current must be limited within the strict bounds established by standards. Otherwise, the manufacturer of front-end converters would not be able to promote a competitive product in the market. The second reason for researching PFC is cost reduction. Although customers require PFC, they are not

willing to pay more for such a function. As a result, a low-cost PFC with good performance indices has become an important issue to power supply manufacturers.

Based on the previous discussion, this dissertation presents an effort towards investigating simple and low-cost solutions for the three-phase PFC used in DPS applications. The main purpose of this dissertation is to devise PFC techniques and circuits for 3kW to 6kW applications that achieve the following features: (1) reduced complexity and (2) reduced cost, while maintaining reasonable performance.

To realize these objectives, chapter 2 discusses the drawbacks and presents improvements to the single-switch discontinuous conduction mode (DCM) rectifier. Analysis, design and experimentation are presented, while an interleaved system using two-channel single-switch DCM boost rectifiers is derived to achieve input current ripple cancellation, and consequently to reduce filtering requirements. Chapter 3 explores a two-switch three-level DCM boost rectifier with improved performance. Because of the voltage stress reduction brought about by using a three-level topology, one can use MOSFETs with low R_{ds-on} to simultaneously increase the switching frequency and efficiency of the PFC circuit. Combining the interleaving technique to cancel the input current ripple with increased switching frequency further reduces input filtering requirements. Another motivation for introducing a two-switch three-level DCM rectifier is to improve the THD of the input current.

In the first part of the dissertation, two-stage approaches are the main focus of the work. Both the single- and two-switch PFC circuits developed in chapters 2 and 3 are interfaced with a high-power three-level DC/DC converter to evaluate the performance of a two-stage approach. All the

comparisons performed in the dissertation are presented against the benchmark circuits previously discussed in this chapter (CCM boost and VIENNA rectifiers).

The second part of this dissertation explores single-stage converters for mainframe computers and servers applications. Two topologies are presented, one of which is further developed to achieve simplified interleaving, thus avoiding the duplication of the entire switching power stage. Chapter 4 presents two novel three-phase single-stage front-end converters implemented for 3kW applications. The motivation for developing single-stage converters is the potential that these approaches present for achieving cost reduction. Both topologies presented in chapter 4 are based on the functional integration of the two-stage approach presented in chapter 3. Three-level topologies are suitable for this type of application because of the voltage stress reduction across the power switches. The first single-stage converter presented in chapter 4 is based on the three-level phase-shift converter, while the second single-stage approach employs an asymmetrical PWM converter to transfer power and to regulate the DC output voltage. Experimental results and comparisons are presented throughout the dissertation to clarify drawbacks and advantages of both single-stage converters, as well as to verify how they stand up against the benchmark circuits and both two-stage approaches developed in chapters 2 and 3.

Chapter 5 is devoted to developing an interleaved single-stage converter that eliminates the need for duplicating the entire switching power stage in order to provide input current ripple cancellation. The features of this technique are analyzed, and experimental results are obtained for a 3kW prototype. Chapter 6 wraps up all the results and summarizes the conclusions drawn from the work developed in this dissertation.

2. Single-Switch Three-Phase DCM Boost Rectifier

2.1. Introduction

Different PFC circuits for DPS applications have been proposed in recent years. For higher power levels (6kW and higher), the need for three-phase rectifiers is clear. However, one of the key practices used by industry to obtain high-power front-end converters is the connection of single-phase power modules to the three-phase AC system, as discussed in section 1.1, and shown schematically in Fig. 2-1(a) [9]-[11]. For a more detailed building block configuration of each power module, refer to Fig. 1-2.

To reduce the cost of the rectifier system, Fig. 2-1(b) shows three single-phase CCM boost rectifiers connected to the same intermediate bus voltage [12]. In this case, the system cost is reduced because only one DC/DC converter is used to regulate the DC output voltage, as opposed to the three DC/DC converters required in Fig. 2-1(a). Nevertheless, connecting the outputs of the rectifiers creates undesirable interactions between the converters. To reduce such interactions, an extra diode is added to each single-phase boost rectifier, while the boost inductor is split into two inductors, as shown in Fig. 1-3. The voltage of the intermediate DC bus must be at least two times higher than the peak line-to-neutral input voltage in order to guarantee proper operation of the CCM boost rectifiers. Although the system shown in Fig. 2-1(b) is simplified with respect to the system illustrated in Fig. 2-1(a), the modularity is lost because the CCM boost rectifiers are connected to the same intermediate bus.

While both approaches for PFC result in high performance, they are high cost because of the circuit complexity and number of components. Therefore, it is clear that lower cost three-phase

PFC circuits are required for high power processing. Having said that, this chapter describes the pros and cons of using discontinuous conduction mode (DCM) boost rectifies for telecom and mainframe computer applications.

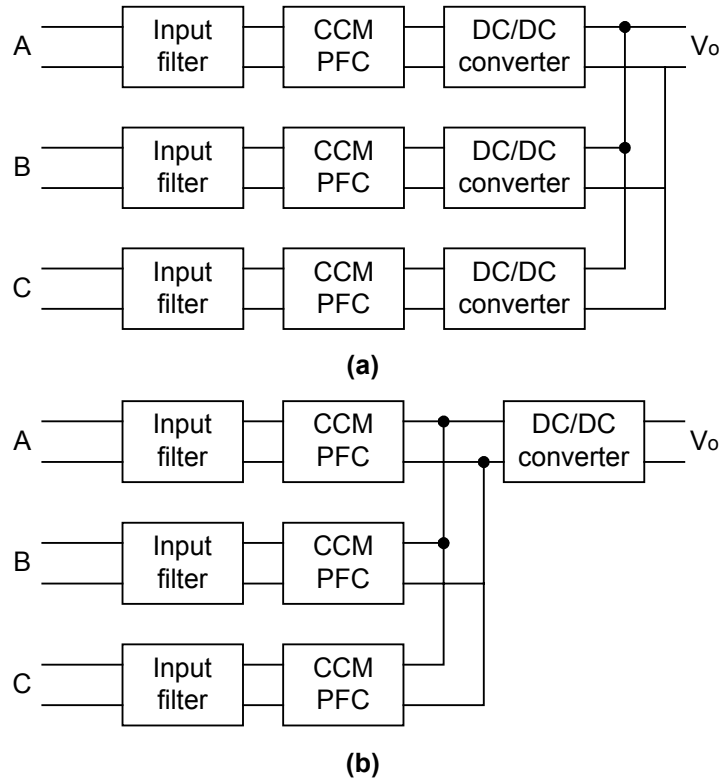


Fig. 2-1. General approach used to obtain PFC for high-power-level applications: (a) single-phase modules and (b) simplified approach.

One of the approaches that can be used to reduce the cost and complexity of the DPS front-end converter for high-power applications is the single-switch three-phase DCM boost rectifier shown in Fig. 2-2 [42]. This topology offers the advantages of simplicity and low harmonic distortion. The following sections are devoted to demonstrating the approaches used to improve the performance of the single-switch DCM boost rectifier.

The main contributions of this chapter are the analysis of the interleaved input current ripple (section 2.5), the analysis of the best switching frequency range to reduce the combined filter and

boost inductors size (section 2.7), and the demonstration of the two-stage approach front-end converter (section 2.8). The analysis of the operation shown in section 2.2 has already been described [43] - [45], and repeated hereafter for the purpose of background information.

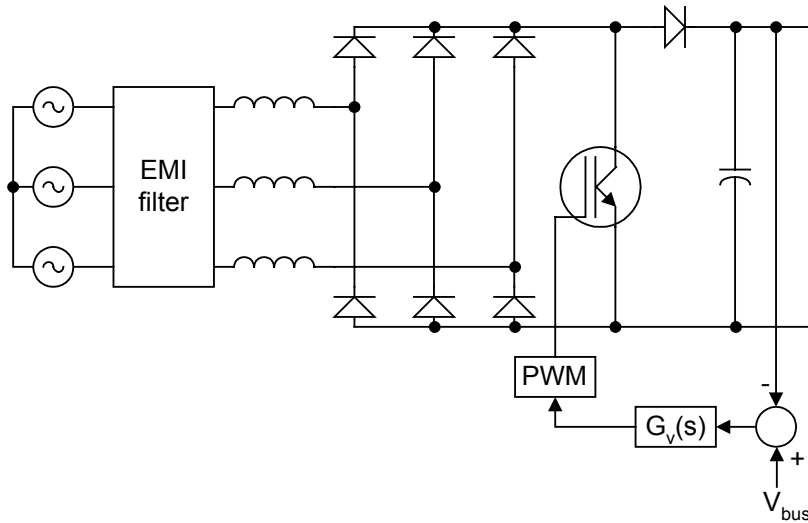


Fig. 2-2. Single-switch three-phase DCM boost rectifier.

2.2. Analysis and Design of the Single-Switch DCM Boost Rectifier

This section provides a simplified analysis and design for the single-switch DCM boost rectifier. Because of the symmetry of three-phase systems, the analysis of the operating stages can be limited to the interval $0 < \theta < \pi/6$. For the purpose of mathematical representation of the DCM boost rectifier operation, the input voltages are assumed to be

$$\begin{aligned}
 v_a &= V_{pk} \sin(\theta) \\
 v_b &= V_{pk} \sin\left(\theta - \frac{2\pi}{3}\right), \\
 v_c &= V_{pk} \sin\left(\theta + \frac{2\pi}{3}\right)
 \end{aligned}
 \tag{2-1}$$

where V_{pk} is the peak input line-to-neutral voltage.

Four operating stages can be identified in a switching period of the single-switch DCM boost rectifier, as shown in Fig. 2-3. In the same figure, k represents the k th switching period within the line period T_r . In the first operating stage, the power switch is turned on to linearly charge the input inductors according to the phase voltage that is applied across each one. In the second operating stage, the power switch is turned off to reset the inductors. The inductor with the lowest peak current resets first. In the third operating stage, the two remaining inductor currents are reset to zero at the same rate. Once the reset interval has finished, the output load is supplied by the energy stored in the output filter capacitor until the next switching period restart. In the analysis that follows, the line-to-neutral input voltage v_a is taken as the reference voltage for the three-phase system established in (2-1).

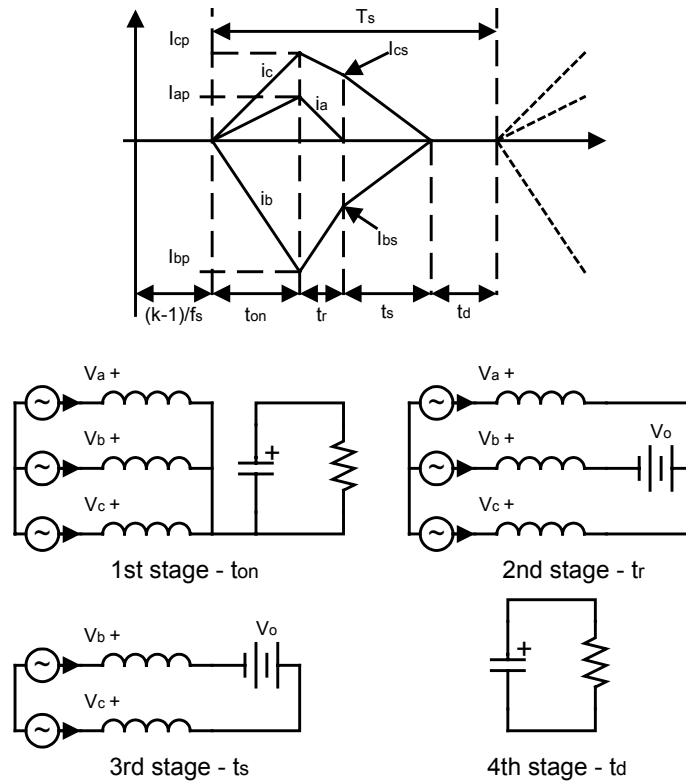


Fig. 2-3. Current in the boost inductors and operating stages in the interval $0 < \theta < \pi/6$ of the input AC voltages.

2.2.1. Average Line Current

The switching frequency of the converter is much higher than the line frequency. Therefore, the line voltages can be considered constant within one switching period. In this case, the peak line currents for a given switching period are given by

$$(2-2) \quad \begin{aligned} I_{ap} &= \frac{v_a D}{L f_s} \\ I_{bp} &= \frac{v_b D}{L f_s}, \\ I_{cp} &= \frac{v_c D}{L f_s} \end{aligned}$$

where the quantities above I_{ap} , I_{bp} and I_{cp} are the peak line currents at the end of the on-time interval, D is the duty cycle, L is the input boost inductance, f_s is the switching frequency, and t_{on} is the on-time switching interval.

To determine the characteristics of the DCM boost rectifier, it is necessary to know the instantaneous average value of the line currents as a function of θ . Once the average line currents have been described within the interval $0 < \theta < \pi/6$, it is then possible to extend the results to the entire line period of the input voltages by using the symmetry properties of three-phase systems. Taking into account the operating stages and the time diagram shown in Fig. 2-3, one can write the expressions of the average line currents for one switching cycle as a function of the phase angle θ , as follows:

$$\begin{aligned}
i_a &= \frac{(t_{on} + t_r)I_{ap}(\theta)}{2T_s} \\
(2-3) \quad i_b &= \frac{t_{on} I_{bp}(\theta)}{2T_s} + \frac{[I_{bs}(\theta) + I_{bp}(\theta)]t_r}{2T_s} + \frac{t_s I_{bs}(\theta)}{2T_s}, \\
i_c &= \frac{t_{on} I_{cp}(\theta)}{2T_s} + \frac{[I_{cs}(\theta) + I_{cp}(\theta)]t_r}{2T_s} + \frac{t_s I_{cs}(\theta)}{2T_s}
\end{aligned}$$

where i_a , i_b and i_c are the average line currents as a function of θ , while I_{bs} and I_{cs} are the currents through lines b and c at the end of the second stage, t_r is the time duration of the second operating stage, t_s is the time duration of the third operating stage, and T_s is the switching period.

The duration of the second stage is the time taken by the current through inductor L_a to be reset:

$$(2-4) \quad t_r = \frac{L(0 - I_{ap})}{v_{La}}.$$

The voltage v_{La} across the inductor connected to line a can be obtained from the equivalent network of the second operating stage, as shown in Fig. 2-3. As a result, the second operating stage provides the following expressions:

$$\begin{aligned}
v_a - v_{La} - V_o + v_{Lb} - v_b &= 0 \\
(2-5) \quad v_a - v_{La} + v_{Lc} - v_c &= 0 \\
v_{La} + v_{Lb} + v_{Lc} &= 0
\end{aligned}$$

Solving the above expressions for the voltage across the input inductors during the second stage results in the following:

$$\begin{aligned}
 v_{La} &= v_a - \frac{V_o}{3} \\
 \text{(2-6)} \quad v_{Lb} &= v_b + \frac{2V_o}{3} \\
 v_{Lc} &= v_c - \frac{V_o}{3}
 \end{aligned}$$

Substituting (2-2) and (2-6) into (2-4), results in the time duration of the second operating stage as a function of output and input voltages, duty cycle and switching frequency:

$$\text{(2-7)} \quad t_r = \frac{D}{f_s} \left[\frac{3v_a}{(V_o - 3v_a)} \right].$$

During the second operating stage, the voltage across the input inductors connected to lines b and c can be obtained from (2-2) and (2-6):

$$\begin{aligned}
 v_{Lb} &= \frac{L(I_{bs} - I_{bp})}{t_r} \\
 \text{(2-8)} \quad v_{Lc} &= \frac{L(I_{cs} - I_{cp})}{t_r}
 \end{aligned}$$

Equations (2-2), (2-6) and (2-7) can be substituted in (2-8). The resulting set of equations can be solved for the current through lines b and c at the end of the second operating stage:

$$\begin{aligned}
 \text{(2-9)} \quad I_{bs} &= \frac{D}{Lf_s} \left[\frac{(v_b + 2v_a)V_o}{V_o - 3v_a} \right] \\
 I_{cs} &= \frac{D}{Lf_s} \left[\frac{(v_c - v_a)V_o}{V_o - 3v_a} \right].
 \end{aligned}$$

It is still necessary to determine the time duration of the third operating stage in order to calculate the average current through the power lines. From Fig. 2-3, the equivalent network of the third operating stage provides the following expressions:

$$(2-10) \quad \begin{aligned} v_b - v_{Lb} + V_o + v_{Lc} - v_c &= 0 \\ v_{Lb} + v_{Lc} &= 0 \end{aligned} .$$

In order to determine the duration of this stage, it is necessary to write down the equation of the voltage applied across inductors L_b or L_c :

$$(2-11) \quad v_{Lb} = -v_{Lc} = \frac{L(0 - I_{bs})}{t_s} .$$

From (2-9), (2-10) and (2-11), one can obtain the expression of the time duration for the third operating stage as follows:

$$(2-12) \quad t_s = \frac{D}{f_s} \left[\frac{-2V_o(2v_a + v_b)}{(V_o - 3v_a)(V_o + v_a + 2v_b)} \right] .$$

From the previous analysis, the average currents through the power lines can be obtained by substituting (2-1), (2-2), (2-7), (2-9) and (2-12) into (2-3). The result is described as follows as a function of the phase angle θ :

$$\begin{aligned}
(2-13) \quad i_a &= \frac{D^2 V_o V_{pk}}{2 L f_s} \left[\frac{\sin(\theta)}{V_o - 3 V_{pk} \sin(\theta)} \right] \\
i_b &= \frac{D^2 V_o V_{pk}}{4 L f_s} \left[\frac{2\sqrt{3} V_{pk} \sin(2\theta) - V_o \sin(\theta) - \sqrt{3} V_o \cos(\theta)}{(V_o - 3 V_{pk} \sin(\theta))(V_o - \sqrt{3} V_{pk} \cos(\theta))} \right] \\
i_c &= \frac{D^2 V_o V_{pk}}{4 L f_s} \left[\frac{-\sqrt{3} V_{pk} \sin(2\theta) - V_o \sin(\theta) + \sqrt{3} V_o \cos(\theta)}{(V_o - 3 V_{pk} \sin(\theta))(V_o - \sqrt{3} V_{pk} \cos(\theta))} \right]
\end{aligned}$$

Equation (2-13) is not normalized, and for this reason it restricts the value of the analysis. The normalized version of (2-13) is given in the following set of expressions:

$$\begin{aligned}
(2-14) \quad i_{an}(\theta) &= \frac{D^2 M}{2} \left[\frac{\sin(\theta)}{(M - 3 \sin(\theta))} \right] \\
i_{bn}(\theta) &= \frac{D^2 M}{2} \left[\frac{\sqrt{3} \sin(2\theta) - M \sin\left(\theta + \frac{\pi}{3}\right)}{(M - 3 \sin(\theta))(M - \sqrt{3} \cos(\theta))} \right], \\
i_{cn}(\theta) &= \frac{D^2 M}{2} \left[\frac{-\frac{\sqrt{3}}{2} \sin(2\theta) - M \sin\left(\theta - \frac{\pi}{3}\right)}{(M - 3 \sin(\theta))(M - \sqrt{3} \cos(\theta))} \right]
\end{aligned}$$

where:

$$\begin{aligned}
(2-15) \quad M &= \frac{V_o}{V_{pk}} \\
\langle i_{an} \quad i_{bn} \quad i_{cn} \rangle &= \frac{\langle i_a \quad i_b \quad i_c \rangle L f_s}{V_{pk}}
\end{aligned}$$

In the expression above, M is the voltage conversion ratio of the single-switch three-phase DCM boost rectifier, while i_{an} , i_{bn} and i_{cn} are the normalized instantaneous average currents through the power lines a, b and c, respectively.

The analysis performed in the first 30° interval of the input line voltages can be extended to the entire line period. Because of the symmetry of the three-phase system, it is enough to expand the analysis of the converter up to one quarter of the line period, as shown in Table 2-1. By phase-shifting the expressions given in (2-14), one can extrapolate the average line currents to the entire line period.

Table 2-1. Extending the results given in (2-14) to one quarter of the line period.

Line	Current During Interval: $0 < \theta < \frac{\pi}{6}$	Current During Interval: $\frac{\pi}{6} < \theta < \frac{\pi}{3}$	Current During Interval: $\frac{\pi}{3} < \theta < \frac{\pi}{2}$
A	$i_{an}(\theta)$	$i_{cn}\left(\frac{\pi}{3} - \theta\right)$	$-i_{bn}\left(\theta - \frac{\pi}{3}\right)$
B	$i_{bn}(\theta)$	$i_{bn}\left(\frac{\pi}{3} - \theta\right)$	$-i_{cn}\left(\theta - \frac{\pi}{3}\right)$
C	$i_{cn}(\theta)$	$i_{an}\left(\frac{\pi}{3} - \theta\right)$	$-i_{an}\left(\theta - \frac{\pi}{3}\right)$

2.2.2. Critical Conduction

It is important to know the boundary between the continuous and discontinuous operating modes so that the converter is designed to operate in DCM under all possible operating conditions. In DCM operation, the currents in the boost inductors are zero before the power switch is turned on again. The total time for which there is current circulating in the input lines can be determined from Fig. 2-3:

$$(2-16) \quad \Delta t = t_{on} + t_r + t_s.$$

Substituting equations (2-1), (2-7) and (2-12) in the expression above results in:

$$(2-17) \quad \Delta t = \frac{DV_o}{f_s} \left[\frac{1}{V_o - \sqrt{3} V_{pk} \cos(\theta)} \right].$$

When the converter operates in critical conduction mode, the time interval described above reaches its maximum value. To determine the phase angle θ at which the time interval in (2-17) reaches its maximum, the derivative of that expression must be taken with respect to θ , as follows:

$$(2-18) \quad \frac{d\Delta t}{d\theta} = \frac{DV_o}{f_s} \left[\frac{-\sqrt{3} V_{pk} \sin(\theta)}{(V_o + \sqrt{3} V_{pk} \cos(\theta))^2} \right].$$

The time interval in (2-17) reaches its maximum when the derivative in (2-18) equals zero, which happens at $\theta=0$. Therefore, the maximum time interval given by (2-17) is:

$$(2-19) \quad \Delta t_{\max} = \frac{DV_o}{f_s} \left[\frac{1}{V_o - \sqrt{3} V_{pk}} \right].$$

It is clear that the Δt_{\max} cannot be greater than the switching period T_s of the boost rectifier. As a result, substituting $\Delta t_{\max}=T_s$ in (2-19) and normalizing it results in:

$$(2-20) \quad M_{cr} = \frac{\sqrt{3}}{1-D},$$

where M_{cr} is the critical value of the voltage conversion ratio that forces the converter to operate in the boundary between the continuous and discontinuous modes. For a given duty cycle, the converter is said to be operating in DCM if $M > M_{cr}$.

2.2.3. Output Characteristics

The output characteristics are a set of curves used to design the DCM boost rectifier, as they represent the voltage conversion ratio as a function of the normalized average output current. To plot the output characteristics, it is necessary to obtain first the output average current. From the topology of the single-switch boost rectifier shown in Fig. 2-2, it can be verified that the average output current equals the average current through the output diode. In the first 30° interval of the line period that has been previously analyzed, the average current through the power rectifier, as a function of the phase angle θ , can be determined as

$$(2-21) \quad i_d = \frac{(I_{bs} + I_{bp})t_r}{2T} + \frac{t_s I_{bs}}{2T}.$$

Substituting (2-1), (2-2), (2-7), (2-9) and (2-12) into (2-21) yields:

$$(2-22) \quad i_d = \frac{3}{4} \frac{(DV_{pk})^2}{L f_s} \left[\frac{V_o - \sqrt{3} V_{pk} \cos(\theta) + \sqrt{3} V_{pk} \cos(\theta)^3 - 3 V_{pk} \sin(\theta) \cos(\theta)^2}{(V_o - 3 V_{pk} \sin(\theta)) (V_o - \sqrt{3} V_{pk} \cos(\theta))} \right].$$

The normalized average current through the output diode as a function of the phase angle θ is then given by

$$(2-23) \quad i_{dn} = \frac{3}{4} D^2 \left[\frac{M - \sqrt{3} \cos(\theta) + \sqrt{3} \cos(\theta)^3 - 3 \sin(\theta) \cos(\theta)^2}{(M - 3 \sin(\theta)) (M - \sqrt{3} \cos(\theta))} \right].$$

The normalization of the output average current follows (2-15). The frequency of the average current through the output diode is six times greater than the line frequency. Therefore, in order to describe a complete period of the average current through the output diode, the analysis only needs to be extended to $\theta=\pi/3$, as shown in Table 2-2.

Table 2-2. Normalized average current through the output diode as a function of phase θ .

Interval	Normalized Average Current
$0 < \theta < \pi/6$	$i_{dn}(\theta)$
$\pi/6 < \theta < \pi/3$	$i_{dn}(\pi/3 - \theta)$

To determine the output average current for one line period, the following integral must be solved:

$$(2-24) \quad I_{on} = \frac{3}{\pi} \left[\int_0^{\pi/6} i_{dn}(\theta) d\theta + \int_{\pi/6}^{\pi/3} i_{dn}(\pi/3 - \theta) d\theta \right].$$

The solution of (2-24) is plotted in Fig. 2-4, and represents the output characteristics. As can be observed, the voltage conversion ratio M is plotted as a function of the normalized average output current I_{on} , using the duty cycle D as the running parameter. The curve that limits the output characteristics is the boundary between the continuous and discontinuous modes. The converter must be designed to operate inside the discontinuous mode of operation to guarantee low harmonic distortion of the input current. As can be seen, the curves are rather steep, which gives a current source characteristic to the single-switch three-phase DCM boost rectifier. His characteristic enables parallel operation without the need to impose current sharing.

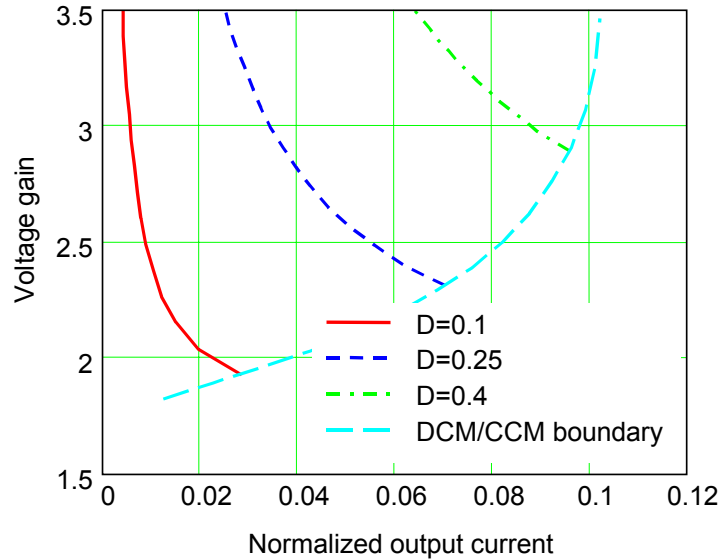


Fig. 2-4. Output characteristics of the single-switch three-phase DCM boost rectifier.

2.2.4. Design Example

This section describes the design of the DCM boost rectifier. In this example, the RMS line-to-neutral input voltage ranges from 187V to 244V, the DC output voltage is 800V, the switching frequency is 40kHz, the output power is 4kW, and the minimum power is 600W (the minimum power could be lower if necessary). From these specifications and from (2-15), the voltage gain M of the DCM boost rectifier is 3.03 at low-line input voltage and 2.32 at high-line. As shown in Fig. 2-5(a), the rectifier is designed at high-line input voltage, and the design point is chosen near the DCM/CCM boundary. This procedure optimizes the design of the DCM boost rectifier by reducing the current stress in the components of the circuit. From the design point shown in Fig. 2-5(a), one can read the output normalized current as 0.065, which is combined with (2-15) and given specifications to result in a boost inductance of 112 μ H. For this particular design, the highlighted area inside the output characteristics seen in Fig. 2-5(a) defines the operating region of the DCM boost rectifier. To obtain low-input-current harmonic distortion, it is necessary to keep the boost rectifiers running in DCM. The duty cycle variation as a function of the

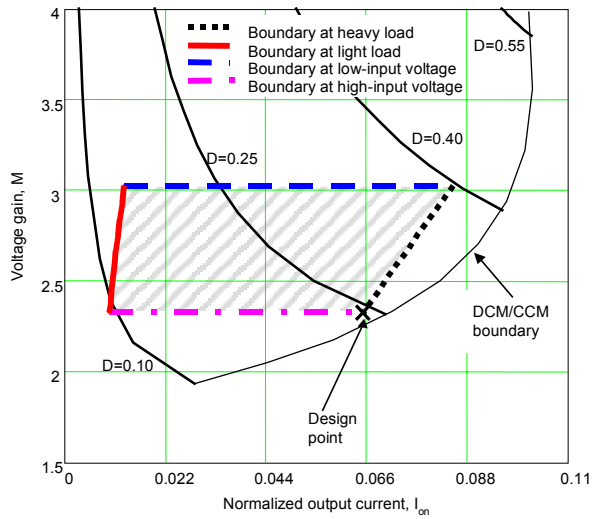
normalized output current is shown in Fig. 2-5(b), while Fig. 2-5(c) illustrates the duty cycle as function of the normalized voltage gain.

2.3. Harmonic Distortion of the Input Currents

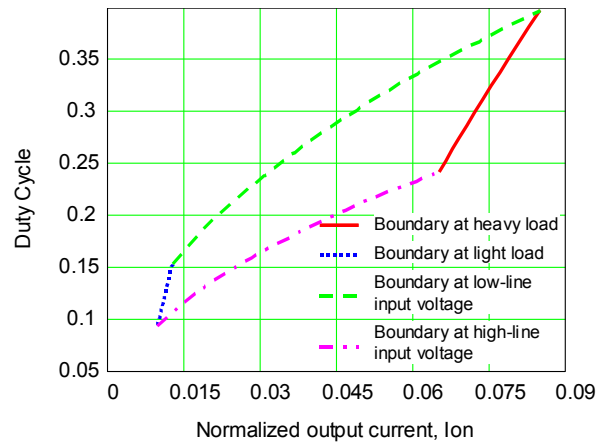
The IEC 61000-3-2 Class A standard limits the emission of harmonics generated by electronic equipment with phase current of up to 16A and 230V of input line-to-neutral voltage [6]. For higher-power equipment with phase currents higher than 16A, the recommendations established in the IEC 61000-3-4 should be used instead [7]. Throughout this work, reference is made only to the IEC 61000-3-2 harmonic standard because the line current is lower than 16A.

In the single-switch three-phase DCM boost rectifier, the fifth harmonic of the input current is the dominant low-frequency harmonic, which is responsible for limiting the power that can be extracted from the rectifier shown in Fig. 2-2, while still meeting the limits of the IEC standard.

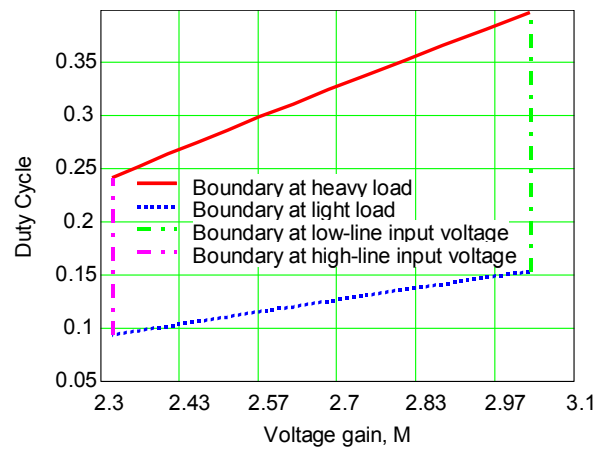
Because of the input current harmonic distortion, the circuit shown in Fig. 2-2 cannot comply with the IEC 61000-3-2 Class A harmonic standard at higher power levels (>6kW at 800V of bus voltage and 220V of line-to-neutral input voltage). To comply with the IEC standard at several kilowatts, the bus voltage of the DCM boost rectifier V_{bus} should be increased. This is not a desirable solution because it will increase the voltage stress across the power devices of the rectifier itself, as well as across the devices of the converter that will be connected across the output of the DCM rectifier.



(a)



(b)



(c)

Fig. 2-5. (a) Operating region of the specified design, (b) duty cycle operating region versus normalized output current, and (c) duty cycle operating region versus voltage gain.

To alleviate this problem to some extent, different modulation techniques have been proposed to reduce the harmonic distortion of the input currents without increasing the bus voltage beyond practical levels. The first approach proposed to improve the harmonic distortion of the input currents involved operating the single-switch boost rectifier in the critical mode [44] [45]. To do this, the power switch must be turned on at the instant at which the boost diode current reaches zero. As a result, the switching frequency is variable, and the effective duty cycle modulation over the line cycle results in reduced THD of the input currents. The drawback of operating the

DCM boost rectifier in the critical mode is the wide switching frequency variation that depends upon both load and input voltage limits.

Another approach for improving the THD of the input current involves controlling to a constant level the average current in the boost diode [46]. In order to keep the average current constant through the boost diode, the duty cycle must be modulated over the line cycle, resulting in an improved input current waveform. The drawback of this method is the extra current sensor required to control the average boost diode current.

A simple technique that can be used to reduce the harmonic distortion of the input current is the so-called harmonic injection method [47]. This method is illustrated in Fig. 2-6(a), and the principles for achieving optimal harmonic injection are described in other work [47]. Fig. 2-6(a) shows that a modulating signal is added to the control signal in order to modulate the duty cycle over the line period. The modulating signal is a sixth-order harmonic signal using an appropriate phase angle extracted from the three-phase input voltages. By controlling the modulation index, it is possible to improve the THD of the input currents. Fig. 2-6(b) shows the effect of the harmonic injection on the spectrum of input currents. As can be observed, when the DCM boost rectifier operates at 8kW of output power and with a constant duty cycle over the line period, the fifth-order harmonic is well above the limit specified by the IEC 61000-3-2 Class A standard. However, under the same operating conditions, the harmonic injection method is able to lower the amplitude of the fifth-order harmonic to slightly below the limit, while still maintaining the same bus voltage. Fig. 2-6(c) shows how the harmonic injection technique helps the boost rectifier comply with the IEC standard at higher power levels. For 800V bus voltage and constant duty cycle control, the maximum power that can be extracted from the DCM boost rectifier is

6kW at 220V line-to-neutral input voltage. At the same bus voltage and the same input phase voltages, the harmonic injection technique increases the power limit to more than 8kW, while still complying with the IEC standard. Therefore, the harmonic injection helps to increase the power level that can be extracted from the DCM boost rectifier without exceeding the limits of harmonic emissions established by the IEC 61000-3-2 Class A standard, while avoiding increasing the bus voltage beyond practical levels.

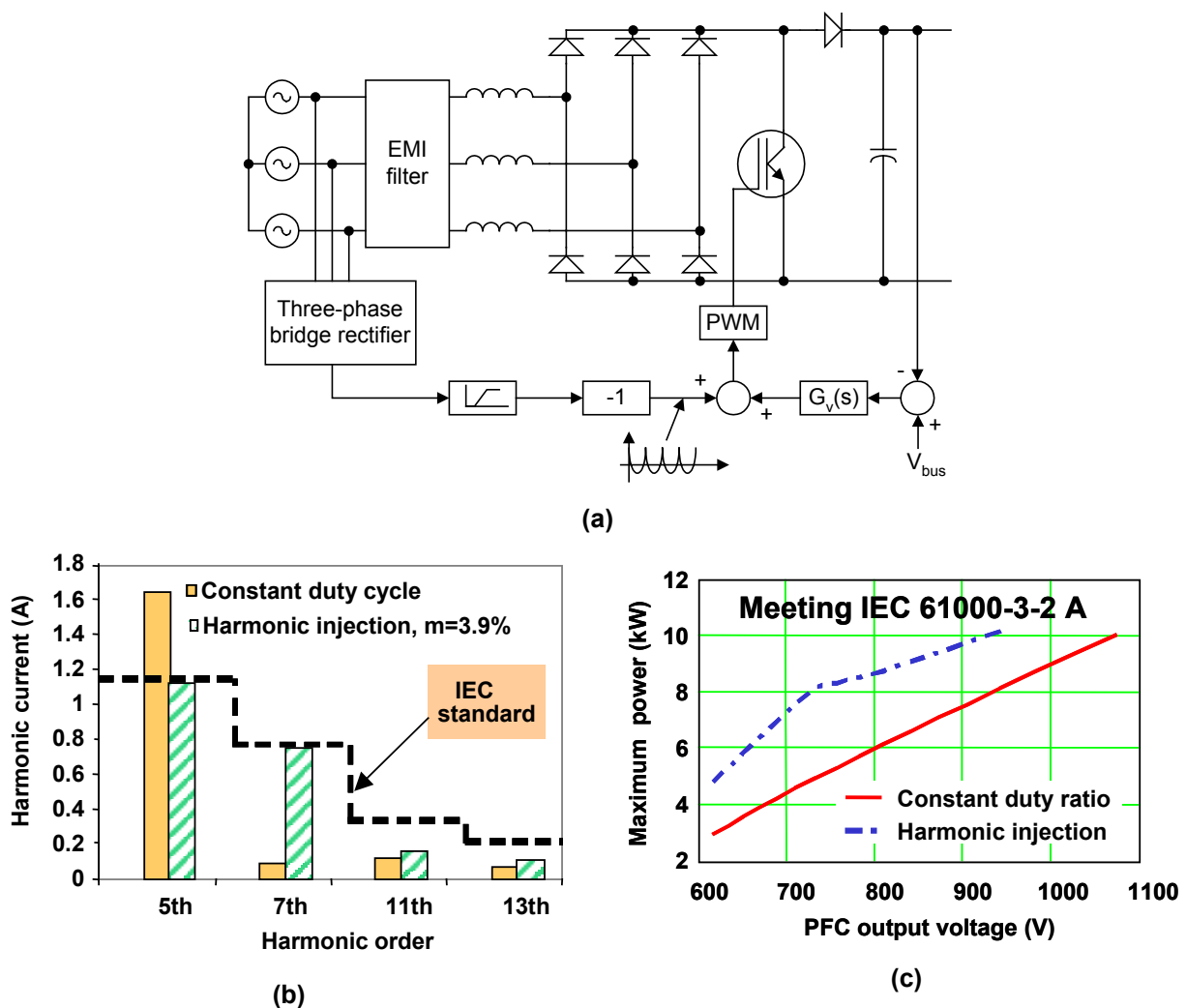


Fig. 2-6. Three-phase DCM boost rectifier: (a) harmonic injection method, (b) harmonic currents at 220V (LN input voltage), 800V of bus voltage and 8kW of output power, and (c) benefit of harmonic injection.

2.4. Impact of DCM Operation on the Input Current Ripple

Due to the DCM operation of the power stage, the current ripple in the input boost inductors is quite large, as compared to those of CCM rectifiers. A higher input current ripple requires a larger input filter, which increases the rectifier cost.

To show the impact of the DCM operation on the amplitude of the high-frequency input current ripple, Fig. 2-7 compares the high-frequency spectrum of the input currents for three different cases: (1) single-phase CCM boost rectifier; (2) VIENNA rectifier; and (3) single-switch three-phase DCM boost rectifier. Cases (1) and (2) refer to the benchmark circuits described in chapter 1 as the baselines for comparison throughout this dissertation. Table 2-3 summarizes the system parameters used in the comparison. As can be verified, all cases draw the same power per phase at the same switching frequency. The boost inductances of the CCM rectifiers (single-phase CCM boost and VIENNA) were designed to limit the maximum peak-to-peak input current ripple to below 25% of the fundamental input peak current value. The bus voltage in all cases is chosen accordingly to allow proper operation. The system parameters used for the DCM boost rectifier follow the design developed in section 2.2.4, except that the power is twice as high and for that reason, the boost inductance is half of that described in section 2.2.4.

Table 2-3. System parameters.

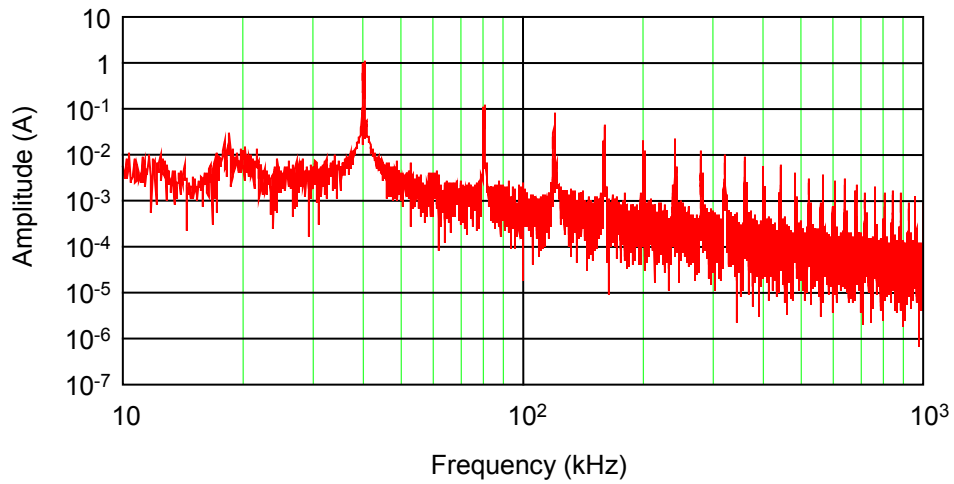
System	Power (kW)	L (μ H)	V_{bus} (V)	f_s (kHz)	V_{in} (V) Line-to-Neutral
Single-Phase CCM Boost Rectifier	2.67 (Need three rectifiers to supply 8kW)	496	400	40	187
VIENNA Rectifier	8	496	800	40	187
Single-Switch DCM Rectifier	8	56	800	40	187

As shown in Fig. 2-7, the high-frequency spectra generated by the single-phase CCM and VIENNA rectifiers are approximately the same. For both cases, the amplitude of the first high-frequency harmonic is 1.1A. However, one can see that the DCM boost rectifier generates more than 10A at 40kHz. Therefore, if the EMI filter were to be designed to limit the emission of high-frequency noise according to the VDE 0871 Class B standard, the size of the input filter needed for the DCM boost rectifier would be much larger than the filter size required to attenuate the noise generated by the CCM rectifiers. To overcome this drawback, an alternative solution for reducing the amplitude of the high-frequency spectrum generated by the DCM rectifier is to interleave the operation of two or more converters, as addressed in the next section.

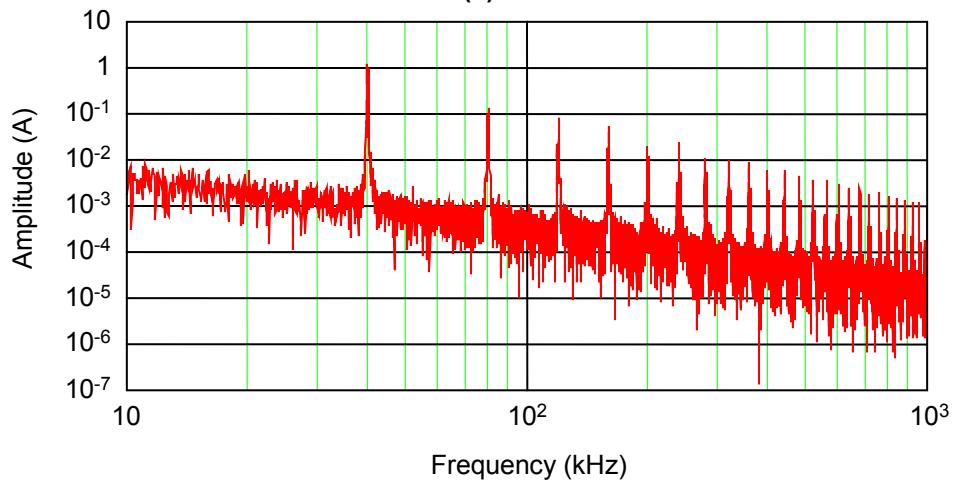
2.5. Interleaved DCM Boost Rectifiers

The EMI noise generated by the input current ripple of the DCM boost rectifier must comply with standards that limit high-frequency conducted noise emissions in electronic equipment. In order to attenuate and limit the ripple of the input current to levels below the specifications of any given EMI standard regulation, an EMI filter must be used at the input of the DCM boost rectifier.

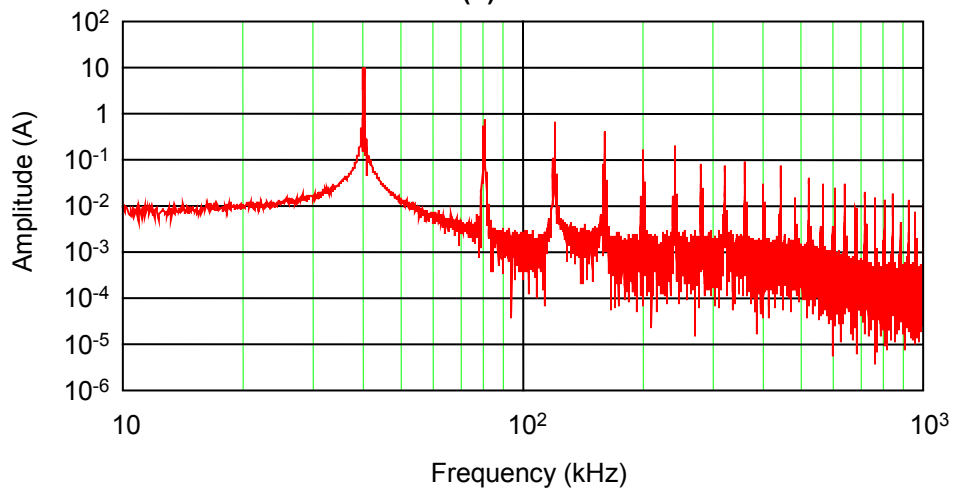
The fundamental component of the high-frequency spectrum of the input current ripple for interleaved rectifiers is centered on the switching frequency, more specifically at the side-band frequencies $f_s \pm f_r$ (f_s is the switching frequency and f_r is the line frequency). Therefore, the cutoff frequency of the EMI filter must be chosen to be well below the switching frequency of the DCM boost rectifier in order to provide appropriate noise attenuation. As a result, the EMI filter connected at the input of the DCM boost rectifier becomes large, since its cutoff frequency is set well below the switching frequency, and the ripple to attenuate is also high.



(a)



(b)



(c)

Fig. 2-7. High frequency spectrum of the input current ripple: (a) single-phase CCM boost rectifier, (b) VIENNA rectifier, and (c) single-switch three-phase DCM boost rectifier.

There are several solutions for overcoming the amplitude spectrum of the input current ripple generated by DCM boost rectifiers. For instance, the critical mode of operation can also be used to reduce the high-frequency amplitude spectrum of the input current ripple [44]. In critical conduction mode, the frequency is modulated according to the amplitude of the AC input voltages and output load. As a consequence of the frequency modulation, the fundamental component of the input current ripple is no longer centered at a single frequency, but is instead spread across the minimum and maximum values of the modulated switching frequency [48]. Therefore, the high-frequency amplitude spectrum of the input current ripple is reduced, which in turn will reduce the size of the EMI input filter. Frequency modulation is beneficial in reducing the amplitude spectrum of the input current ripple, but this technique complicates the design of magnetic devices, increases the switching losses at high switching frequencies, and requires auxiliary circuitry to keep the converter running in critical mode. To simplify this approach while reducing the input current ripple, one can interleave the operation of two or more constant-frequency DCM boost rectifiers [49]-[51]. Interleaved rectifiers are able to reduce the amplitude of the input current ripple and increase the effective ripple frequency according to the number of interleaved channels. A drawback of interleaving the converters is that the number of components used in the system must be increased according to the number of interleaved channels. Therefore, in order to maintain the low cost, the number of interleaved channels cannot be high. Although the interleaving technique increases the number of components, the device current ratings are reduced by a factor that depends upon the number of interleaved converters.

Fig. 2-8 shows the schematic representation of a two-channel interleaved system. Diodes D_{10} and D_{20} have been added to the power stage in order to eliminate electrical interactions between the rectifiers. The drawback of adding diodes D_{10} and D_{20} is that the gate signals require isolation.

To provide appropriate interleaving, the gate signals must be phase-shifted by 180° . Phase-shifting the gate signals also phase-shifts the input inductor currents connected to the same phase. Therefore, the effective line current, which is the sum of the inductor currents connected to the same phase, will present a lower input current ripple. Additionally, the dominant high-frequency harmonic of the interleaved input current is not centered around f_s , but around nf_s , where n is the number of interleaved channels and f_s is the switching frequency.

As a result of the reduced input current ripple and incremental increase in the effective ripple frequency, the EMI filter can be designed with a higher cutoff frequency and lower attenuation, as compared to the case using a single rectifier. Consequently, the size of the DM input filter is also reduced. In addition to reducing the size of the EMI input filter, the interleaving of boost converters can also increase the overall power level of the rectifier system by sharing the total power between the interleaved rectifiers. Despite these advantages, the interleaving technique cannot improve the low-frequency harmonic content characteristic of the boost converters operated in DCM, as demonstrated in the next section.

2.5.1. Analysis of the Interleaved Input Current Ripple

This section presents the analysis of the interleaved input current ripple using a frequency domain technique. The results of this analysis can be used to design the DM input filter [52]. Fig. 2-3 shows the high-frequency boost inductor currents for one switching period, sampled in the interval $0 < \theta < \pi/6$ of the AC input voltages. According to the operating stages of the DCM boost rectifiers, and the timing diagram for one switching period as illustrated in Fig. 2-3, it is possible

to write all equations that define the generic high-frequency current triangles for each phase, as summarized in Table 2-4.

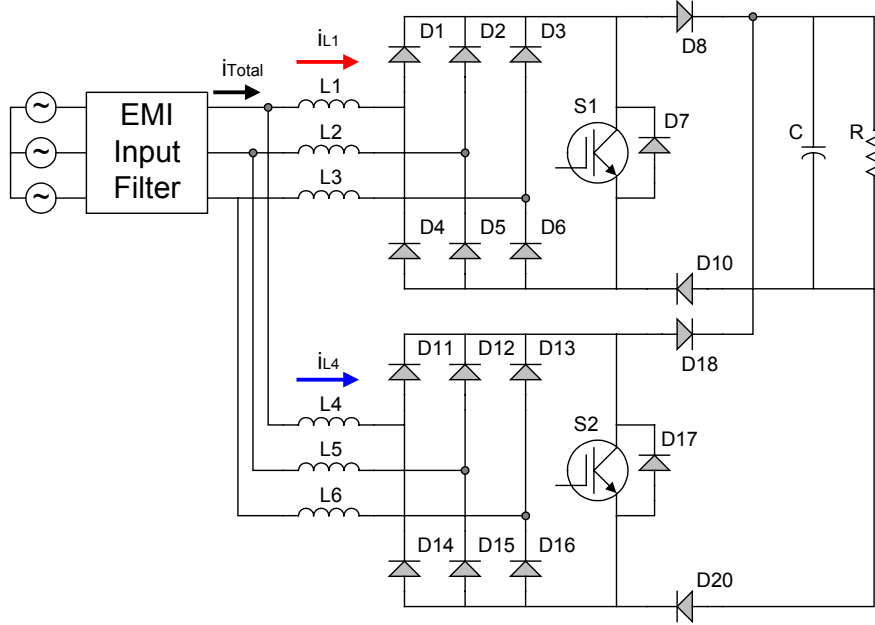


Fig. 2-8. Two interleaved DCM boost rectifiers.

The phase angle θ in Table 2-4 is given by

$$(2-25) \quad \theta = (k-1) \frac{\pi/6}{p-1}, \quad k = 1, 2, \dots, p,$$

where p is the number of high-frequency triangles that can fit into the interval $0 < \theta < \pi/6$ of the AC input voltages, and k represents the k th triangle sampled in that interval.

The boost inductor current is periodical, and for this reason it can be represented by the Fourier series, as follows:

$$(2-26) \quad i_a(t) = C_o + 2 \sum_{m=1}^{\infty} \left| \frac{1}{T_r} \int_0^{T_r} i_a(t) e^{-j\omega t} dt \right| \cos(\omega t - \theta_m),$$

where $\omega = m\omega_r = 2\pi m f_r$. The variable m is the harmonic order of the line current, f_r is the line frequency, and T_r the line period.

As mentioned above, it is assumed that an integer number of high-frequency triangles can fit into one line period. Therefore, the integral in (2-26) can be rewritten as

$$(2-27) \quad i(t) = C_o + 2 \sum_{m=1}^{\infty} \left| \frac{1}{T_r} \left(\int_0^{T_s} i_{\Delta_1}(t) e^{-j\omega t} dt + \int_{T_s}^{2T_s} i_{\Delta_2}(t) e^{-j\omega t} dt + \dots + \int_{(v-1)T_s}^{vT_s} i_{\Delta_v}(t) e^{-j\omega t} dt \right) \right| \cos(\omega t - \theta_m), \quad v = 1, 2, \dots, 12p.$$

Equation (2-27) can be further simplified to

$$(2-28) \quad i(t) = C_o + \sum_{m=1}^{\infty} \left| 2 f_r \sum_{v=1}^{\frac{T_r}{T_s}=12p} F_v(j\omega) \right| \cos(\omega t - \theta_m),$$

where $12p$ is the total number of high-frequency current triangles that can fit into one period of the AC input voltages, and

$$(2-29) \quad F_v(j\omega) = \int_{(v-1)T_s}^{vT_s} i_{\Delta_v}(t) e^{-j\omega t} dt.$$

The current $i_{\Delta_v}(t)$ in (2-29) is the high-frequency boost inductor current for every switching cycle within the line period. From (2-28), the amplitude spectrum of the boost inductor current for one DCM boost rectifier can be written as

$$(2-30) \quad |G(j\omega)| = \left| 2f_r \sum_{v=1}^{\frac{T_r}{T_s}} F_v(j\omega) \right|.$$

Table 2-4. Mathematical representation of the high-frequency inductor currents at different operating stages during the interval $0 < \theta < \pi/6$ of the AC voltages.

Input Phase	1st Stage of Operation $\frac{k-1}{f_s} < t < \frac{k-1}{f_s} + \frac{D}{f_s}$	2nd Stage of Operation $\frac{k-1}{f_s} + \frac{D}{f_s} < t < \frac{k-1}{f_s} + \frac{D}{f_s} + t_r$	3rd Stage of Operation $\frac{k-1}{f_s} + \frac{D}{f_s} + t_r < t < \left(\frac{k-1}{f_s} + \frac{D}{f_s} + t_r + t_s \right)$
A	$i_{a_on}(t) = I_{ap} \frac{f_s}{D} t + \frac{I_{ap}}{D} (1-k)$ $I_{ap} = \frac{V_a D}{L f_s}$ $V_a = V_{pk} \sin(\theta)$	$i_{a_r}(t) = -\frac{I_{ap}}{t_r} t + \frac{I_{ap}(D + t_r f_s + k - 1)}{t_r f_s}$	$i_{a_s}(t) = 0$
B	$i_{b_on}(t) = I_{bp} \frac{f_s}{D} t + \frac{I_{bp}}{D} (1-k)$ $I_{bp} = \frac{V_b D}{L f_s}$ $V_b = V_{pk} \sin\left(\theta - \frac{2\pi}{3}\right)$	$i_{b_r}(t) = -\frac{I_{bp} - I_{bs}}{t_r} t + \frac{I_{bp}(D + t_r f_s + k - 1) - I_{bs}(D + k - 1)}{t_r f_s}$ $I_{bs} = \frac{D}{L f_s} \left(\frac{V_a(2V_o - V_a - V_c) + V_b(V_o + V_b + V_c)}{V_o - 2V_a + V_b + V_c} \right)$	$i_{b_s}(t) = -\frac{I_{bs}}{t_s} t + \frac{I_{bs}(D + (t_r + t_s)f_s + k - 1)}{t_s f_s}$
C	$i_{c_on}(t) = I_{cp} \frac{f_s}{D} t + \frac{I_{cp}}{D} (1-k)$ $I_{cp} = \frac{V_c D}{L f_s}$ $V_c = V_{pk} \sin\left(\theta + \frac{2\pi}{3}\right)$	$i_{c_r}(t) = -\frac{I_{cp} - I_{cs}}{t_r} t + \frac{I_{cp}(D + t_r f_s + k - 1) - I_{cs}(D + k - 1)}{t_r f_s}$ $I_{cs} = \frac{D}{L f_s} \left(\frac{-V_a(V_o + V_a + V_b) + V_c(V_o + V_b + V_c)}{V_o - 2V_a + V_b + V_c} \right)$	$i_{c_s}(t) = -\frac{I_{cs}}{t_s} t + \frac{I_{cs}(D + (t_r + t_s)f_s + k - 1)}{t_s f_s}$
Time Interval	$t_{on} = \frac{D}{f_s}$	$t_r = \frac{3D}{f_s} \frac{V_a}{(V_o - 2V_a + V_b + V_c)}$	$t_s = -\frac{2}{f_s} \left(\frac{V_a(2V_o - V_a - V_c) + V_b(V_o + V_b + V_c)}{(V_o - 2V_a + V_b + V_c)} \right)$

For n interleaved rectifiers, the gate signals are phase-shifted with respect to each other by T_s/n .

Therefore, the amplitude spectrum of the input interleaved current for n interleaved boost rectifiers is given by

$$(2-31) \quad |G_{\text{int}}(\omega)| = \left| G(j\omega) \left(\sum_{i=1}^n e^{-j\omega \frac{i-1}{nf_s}} \right) \right|.$$

The results of the previous analysis can be implemented on a computer algorithm used to calculate the amplitude spectrum of the interleaved input current for any number of interleaved DCM boost rectifiers.

Besides determining the spectrum composition, one must also determine the operating point related to the worst-case ripple condition in order to design the input DM filter parameters. The high-frequency spectrum of the interleaved current is composed of infinite harmonics. However, the dominant high-frequency harmonic of the interleaved input current usually dictates the design of the input DM filter². For n interleaved DCM boost rectifiers, the dominant high-frequency harmonic of the interleaved current occurs at the side-band frequencies $(nf_s \pm f_r)$, which become $(2f_s \pm f_r)$ for two interleaved converters.

Fig. 2-9(a) shows the maximum normalized amplitude of the dominant high-frequency harmonic of the input current for two interleaved DCM boost rectifiers as a function of the voltage gain M . There are two curves represented in Fig. 2-9 for each graph: one is plotted for the design related to the 187V to 244V line-to-neutral input voltage variation, while the other curve is related to the 170V to 265V voltage range. The latter voltage range is more common for three-phase applications. Fig. 2-9(a) was obtained from the previous analysis by fixing the voltage gain and

² This affirmation is true when the VDE 0871 EMI standard is used to design the input filter, since it starts limiting noise at 10kHz. For other standards, such as the EN 55022 (CISPR 22), the situation requires further analysis since the initial frequency limiting noise is 150kHz.

by changing the duty cycle from minimum to maximum, according to the operating region shown in Fig. 2-5(c). By changing the duty cycle from minimum to maximum and fixing the voltage gain, the maximum normalized high-frequency harmonic of the interleaved current can be identified and plotted as shown in Fig. 2-9(a). In a similar fashion, Fig. 2-9(b) represents the operating duty cycle associated with the maximum amplitude of the dominant high-frequency harmonic of the interleaved current shown in Fig. 2-9(a).

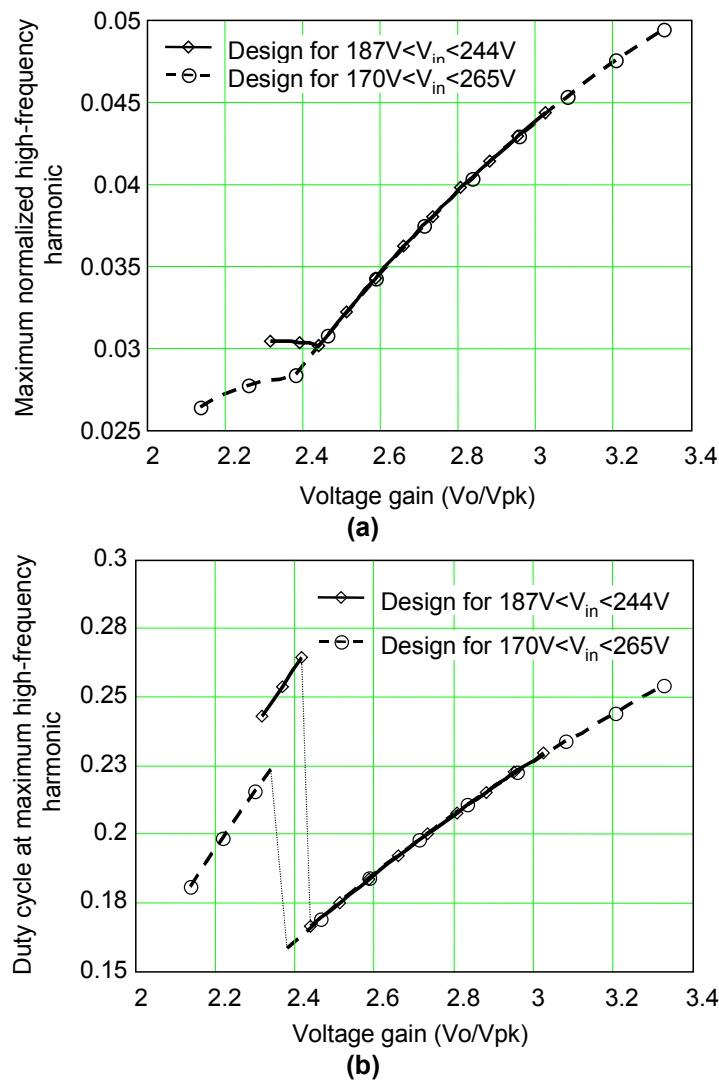


Fig. 2-9. Results of the interleaved current analysis: (a) maximum normalized amplitude of the dominant high-frequency harmonic for two interleaved DCM boost rectifiers and (b) duty cycle associated with the maximum dominant high-frequency harmonic.

For both designs depicted in Fig. 2-9(a), the worst-case ripple condition occurs at low-line input voltage, which is represented by the highest voltage gain. As a result, the DM input filter must be designed at low-line input voltage to guarantee the attenuation of the worst-case interleaved ripple condition. The break point shown in Fig. 2-9(b) occurs because for a specific voltage gain there are two different duty cycles associated with the same maximum amplitude of the dominant high-frequency harmonic. After determining the operating point that leads to this maximum, the results of the previous analysis can be used to calculate the parameters of the DM input filter at the worst-case interleaved input current ripple.

For the design example given in section 2.2.4 (187V to 244V of input voltage variation), the voltage gain at low-line input voltage is 3.03. Taking into account this voltage gain in Fig. 2-9(a), the maximum normalized high-frequency dominant harmonic equals 0.044. From (2-15) and section 2.2.4, the denormalized high-frequency harmonic of the interleaved current results in 2.625A. The duty cycle at which the maximum dominant high-frequency harmonic occurs is 0.235, obtained from Fig. 2-9(b) at low-line input voltage ($M=3.03$).

Fig. 2-10 shows the results obtained when the interleaved system works at the operating point identified in the previous paragraph. Fig. 2-10(a) shows the calculated low-frequency spectrum of the interleaved current, as well as the spectrum of the current produced by a non-interleaved DCM boost rectifier operated at the same power level as the interleaved system. As seen in the figure, the interleaving technique has no effect on the cancellation of low-frequency harmonics. For the same operating point, Fig. 2-10(b) shows the calculated high-frequency spectra of the interleaved and non-interleaved systems at the same output power level. As can be observed, the interleaving technique cancels out the odd high-frequency harmonics of the interleaved input

current. The dominant high-frequency harmonic of the interleaved system occurs at $80\text{kHz} \pm 60\text{Hz}$, whereas for the non-interleaved DCM boost rectifier it occurs at $40\text{kHz} \pm 60\text{Hz}$. Fig. 2-10(c) shows the measured input current for the interleaved system operated at low line (187V) and $D=0.235$ (worst-case interleaved input current ripple condition). To validate the analysis presented in this section, Fig. 2-10(d) compares the experimental and theoretical frequency spectra of the interleaved current at the worst-case ripple condition. The results show very close agreement between theoretical and experimental results, which validates the analysis derived above that is used to predict the amplitude spectrum of the interleaved input current.

2.5.2. Experimental Results

A two-channel interleaved DCM boost rectifier has been implemented for 8kW, as shown in Fig. 2-11(a). Ferrite E55 cores were used to implement the $112\mu\text{H}$ boost inductors, IXSN35N1200U1 IGBTs for the main switches, DSEI 30-10A fast diodes for the rectifiers, and IXTN15N100 MOSFETs for the auxiliary zero-current transition (ZCT) switches. The resonant components of the ZCT circuit were $L_r=5.7\mu\text{H}$ (E21 ferrite core) and $C_r=40\text{nF}/630\text{V}$ (polypropylene capacitor). The design procedure of the ZCT circuit has been described previously [53]. Fig. 2-11(b) and Fig. 2-11(c) show the results obtained from the interleaved system operated at 8kW (4kW per channel). The two upper traces represent the input voltage and filtered input current, while the lower trace is the interleaved current. As can be observed, two-channel interleaved boost rectifiers are quite effective in providing input current ripple cancellation. The effectiveness of reducing the size of the input filter by interleaving the operation of two rectifiers will be addressed in section 2.7.

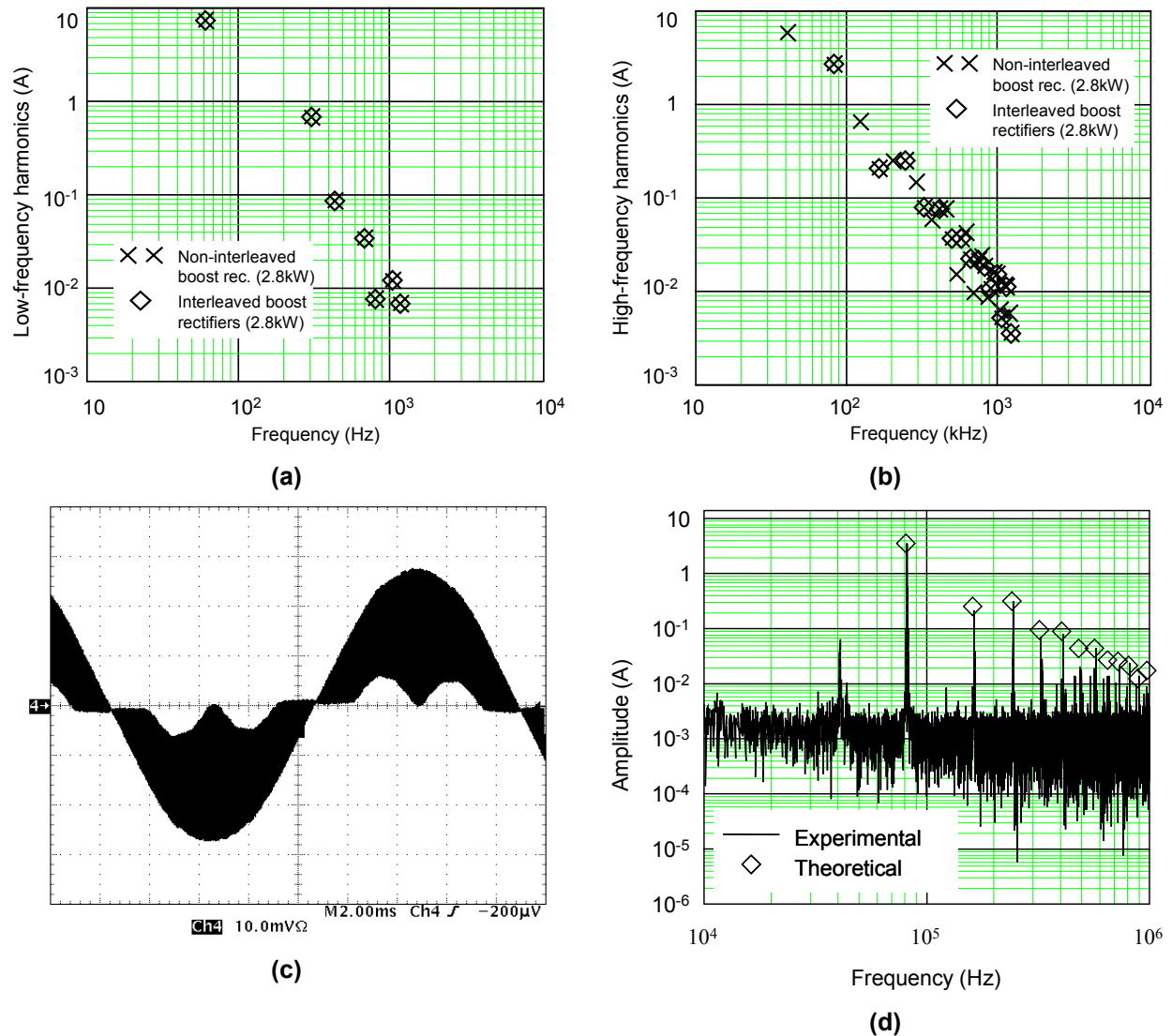


Fig. 2-10. (a) Low-frequency spectrum of the interleaved current at 187V, $D=0.235$, and $P_o=2.8kW$ total, (b) high-frequency spectrum under the same operating condition, (c) experimental interleaved input current at worst-case ripple (5A/div), and (d) comparison between experimental and theoretical spectra.

The harmonics of the input current obtained at 8kW with constant duty cycle modulation do not comply with the IEC 61000-3-2 standard. However, the harmonic injection method is able to improve the THD and help the interleaved system meet the standard. The load sharing between the two interleaved rectifiers is shown in Fig. 2-12(a). The two converters naturally share the load, without requiring current mode control. This result is a consequence of the fact that the DCM boost rectifier has a current source characteristic, which facilitates natural current sharing.

Finally, Fig. 2-12(b) shows the efficiency of the DCM boost rectifier for two different designs. The first design is the same one discussed in section 2.2.4, while the second design was targeted at 6kW of total power using an input line-to-neutral voltage variation of 170V to 265V. At 220V line-to-neutral voltage, the efficiency of the first design was 94.5%, while the second design resulted in 96%. The second design used the same devices, except that the boost inductance was set to 140 μ H.

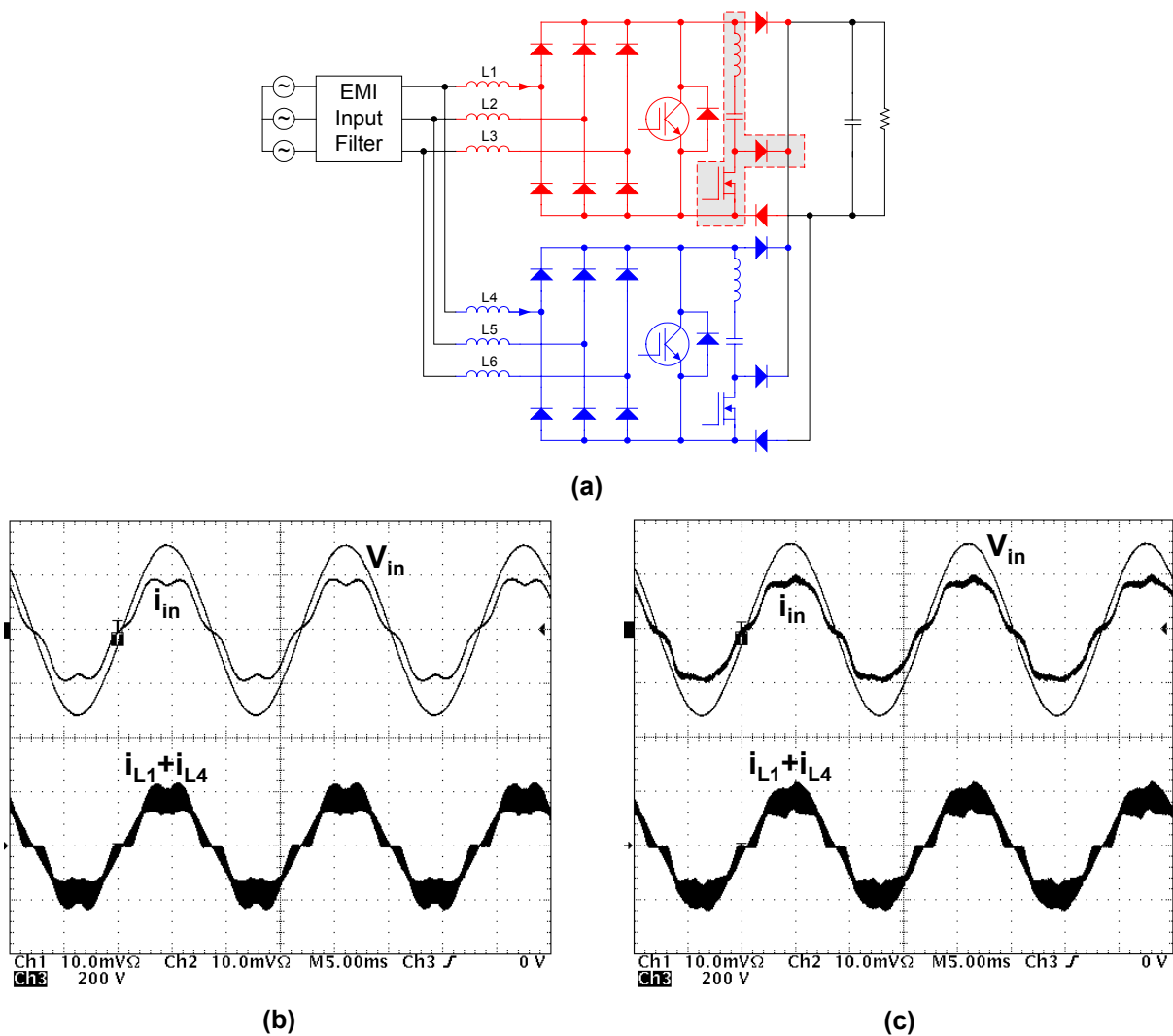
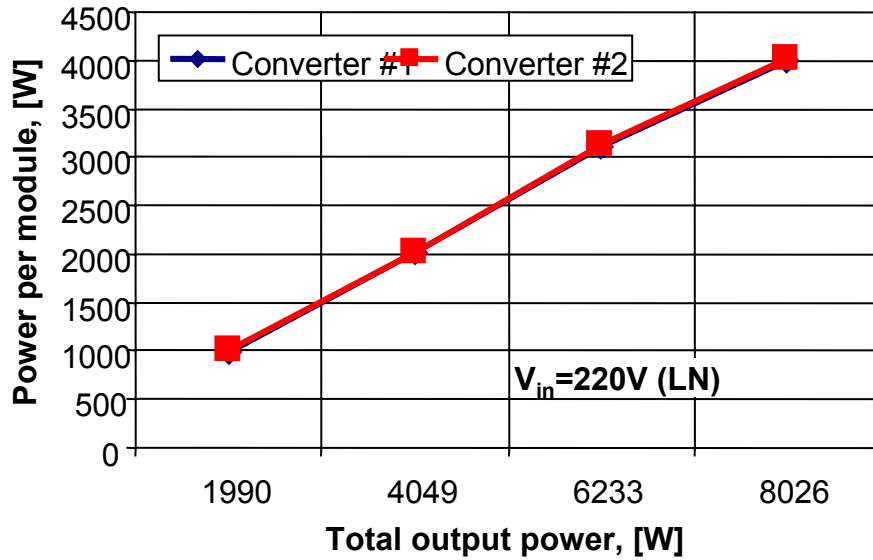
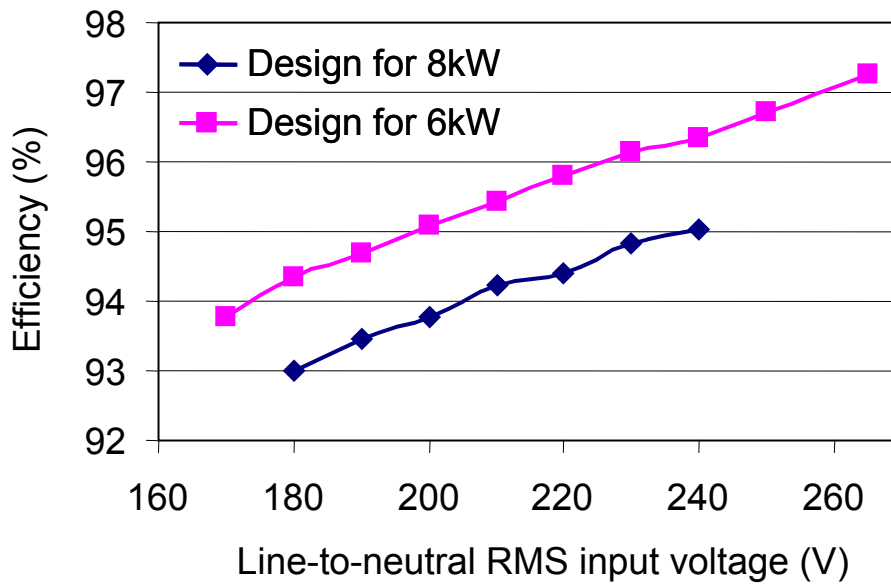


Fig. 2-11. Two-channel interleaved DCM boost rectifiers: (a) configuration, (b) results without harmonic injection at $V_{in}=220$ V (line-to-neutral), $P_o=8$ kW, $f_s=40$ kHz, and $V_o=800$ V (THD=12.7%), and (c) results with harmonic injection (THD=10.8%). All current traces are 20A/div and all voltage traces are 200V/div.



(a)



(b)

Fig. 2-12. (a) Load sharing and (b) efficiency.

2.6. Impact of Control Strategies on the Amplitude Spectrum of the DCM Input Current

This section compares three different control strategies and their effect on the low- and high-frequency spectra of the input current of DCM boost rectifiers [54]. For the purpose of comparison, the operating point of the single-switch DCM boost rectifier is $V_{in}=220V$, $V_o=800V$,

$P_o=4\text{kW}$, $f_s=40\text{kHz}$, and $L=140\mu\text{H}$. The control strategies under consideration, all applied to the single-switch DCM boost rectifier, are (1) fixed switching frequency with fixed duty cycle over the line period, (2) fixed frequency with harmonic injection method, and (3) variable switching frequency.

2.6.1. Low-Frequency Spectrum

Fig. 2-13(a) shows the low-frequency spectrum of the input current for all the control strategies at the operating point defined above. As can be observed, all control strategies produce the same harmonic current at the line frequency, which guarantees that the same power is being delivered to the output in all cases. The fixed duty cycle control produces the highest fifth-order harmonic among all control strategies, which is a major factor limiting the maximum power that can be extracted from the DCM boost rectifier in order to comply with the IEC standard. The harmonic injection method and the variable switching frequency control strategies are able to decrease the magnitude of the fifth harmonic, while increasing the amplitude of the other higher-order harmonics. In fact, the harmonic injection method and the variable switching frequency control shift the energy concentrated at the fifth harmonic to other higher-order harmonics.

2.6.2. High-Frequency Spectrum

Fig. 2-13(b) shows the high-frequency spectrum obtained from the input currents generated by the three control strategies under comparison. As expected, different control strategies produce different high-frequency spectra. The fixed duty cycle control and the harmonic injection method with fixed switching frequency have very similar high-frequency spectra. However, in the upper frequency range the harmonic injection method enables the rectifier to slightly reduce the

harmonics. The variable switching frequency control, however, yields the lowest levels of high-frequency harmonic over the entire frequency range. This control strategy is advantageous for reducing the noise because it spreads out the amplitude spectrum across a range of frequencies.

The conducted noise measurement under standard conditions actually considers a window of frequencies. In this way, the variable frequency control at high frequencies may not exhibit results that are much better than those of the other two fixed frequency control schemes. Fig. 2-13(c) shows the high-frequency spectra when the quadratic sum of the harmonics within a 9kHz window of frequencies is taken into account. Under this assumption, the gain of the harmonics that are inside the sweeping window is unity, while the gain of the harmonics outside the window of frequencies is zero. As a result, when this measurement method is taken into account, the advantage of the variable frequency control becomes less pronounced in the high frequency range.

2.6.3. Effect of Timing Mismatch in Interleaved Rectifiers

The interleaving of DCM boost rectifiers was demonstrated in section 2.5 as an effective technique to eliminate high-frequency harmonics. The effectiveness of the interleaving technique is highly dependent on the phase-shift between the two interleaved rectifiers. Fig. 2-14 illustrates the effect of the phase-shift error on the amplitude of the harmonics concentrated around the switching frequency when two rectifiers are interleaved. If the phase-shift differs $\pm 10\%$ from 180° , the amplitude of the harmonics around the switching frequency already becomes comparable to the amplitude of the dominant high-frequency harmonic, which is centered at $(2f_s \pm f_r)$. As a result, the interleaving of two DCM rectifiers will not be able to eliminate the input

current ripple around the switching frequency if the phase-shift of the gate signals is different from 180° . This effect can be observed in the experimental spectrum of the interleaved current illustrated in Fig. 2-10(d), which shows that despite the interleaving of the two rectifiers, there is still some ripple left at the switching frequency (40kHz).

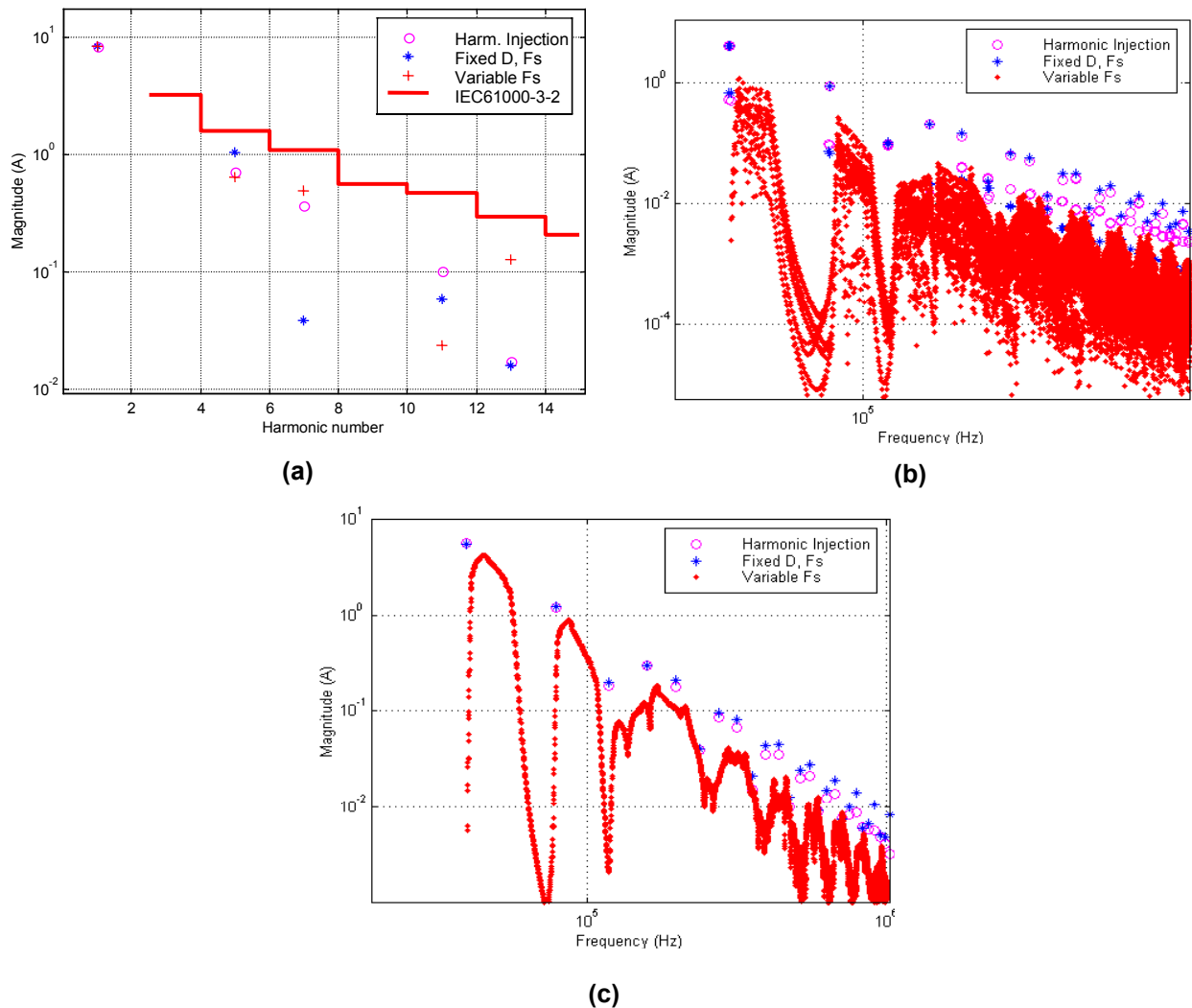


Fig. 2-13. (a) Low-order harmonic comparison, (b) high-frequency spectrum for each control strategy and (c) equivalent high-frequency spectrum when a 9kHz window is considered in the spectrum calculation (quadratic sum).

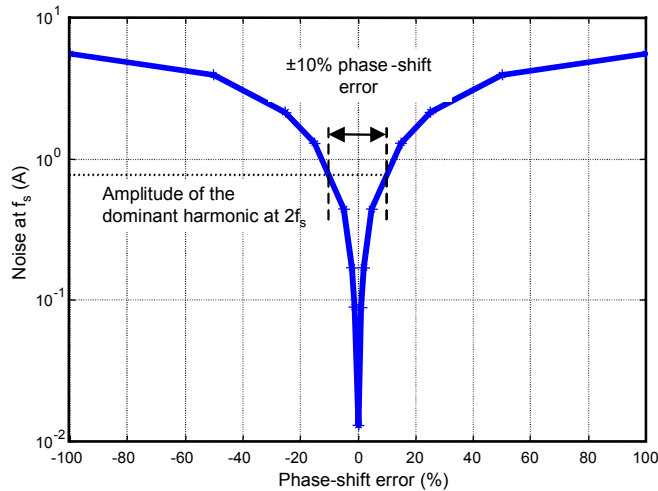


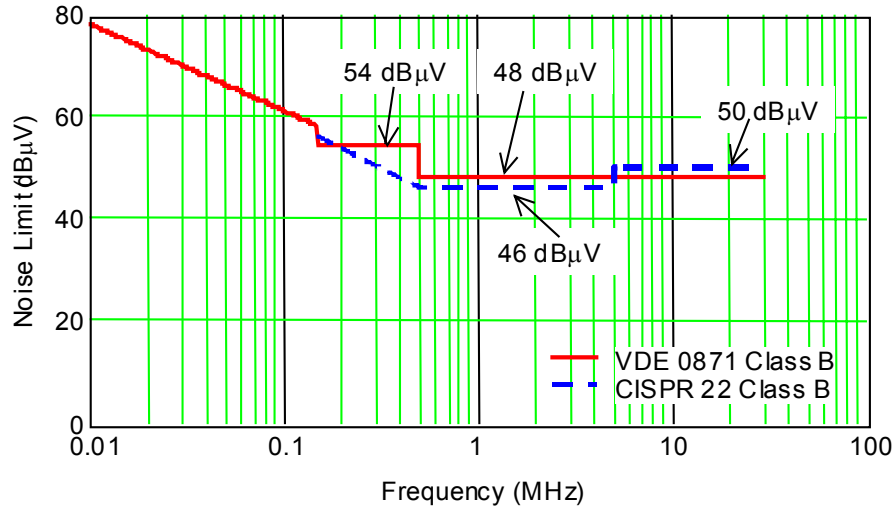
Fig. 2-14. The impact of phase-shift error on the amplitude of the harmonic at the switching frequency for two interleaved rectifiers operated with fixed frequency and fixed duty cycle control.

2.7. DM Filter Parameters and Comparison

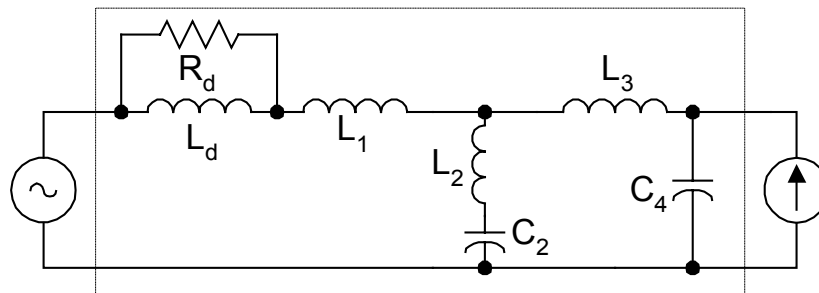
This section provides the DM input filter design and comparison for the following cases: (1) CCM single-phase boost rectifier, (2) VIENNA rectifier and (3) interleaved system. The comparison of DM input filter parameters is provided for two different standards: the VDE 0871 and EN 55022 (CISPR 22), both Class B, as shown in Fig. 2-15(a). The equivalent DM input filter per phase network used in the comparison is shown in Fig. 2-15(b). The filter is a fourth-order Cauer-Chebyshev (CC) network in which R_d is the high-frequency damping resistor and L_d is the low-frequency current bypass inductor used to reduce loss in the damping resistor [56] [57].

The system parameters used in the comparison are summarized in Table 2-5. The total power under consideration and throughout the remainder of this dissertation is 6kW. The same boost inductance was used in both benchmark circuits (CCM boost and VIENNA rectifiers), and was determined to limit the maximum instantaneous peak-to-peak current ripple to below 25% of the fundamental input peak current measured at low-line input voltage and full load. Additionally,

the inductance value of the interleaved system shown in Table 2-5 refers to one of the six inductances used in the configuration illustrated in Fig. 2-11(a).



(a)



(b)

Fig. 2-15. (a) EMI standards for conducted noise (average limits) and (b) equivalent DM filter for one phase.

Table 2-5. System parameters.

System	Power (kW)	L (μ H) @ 40kHz	V _{bus} (V)	V _{in} (V) Line-to-Neutral
Single-Phase CCM Boost Rectifier	2 (Need three rectifiers to supply 6kW)	600	400	170
VIENNA Rectifier	6	600	800	170
Interleaved Single-Switch DCM Rectifiers	6	140 (Per inductance)	800	170

2.7.1. Conducted EMI Simulation Setup for Single- and Three-Phase Converters

To provide a meaningful comparison, it is necessary to emulate as closely as possible the conditions of practical measurements. Therefore, the DM noise characterization follows the measurement setup used for single-phase equipment, as shown in Fig. 2-16. The dotted box represents the line impedance stabilization network (LISN), which is used to provide a well-defined impedance to the noise source generated by the equipment under test (EUT). As can be observed, the LISN output must always be terminated by a 50Ω impedance.

The setup to evaluate the DM EMI noise of three-phase equipment is shown in Fig. 2-17. The result of the simulation in one of the three phases is used to design the DM filter parameters.

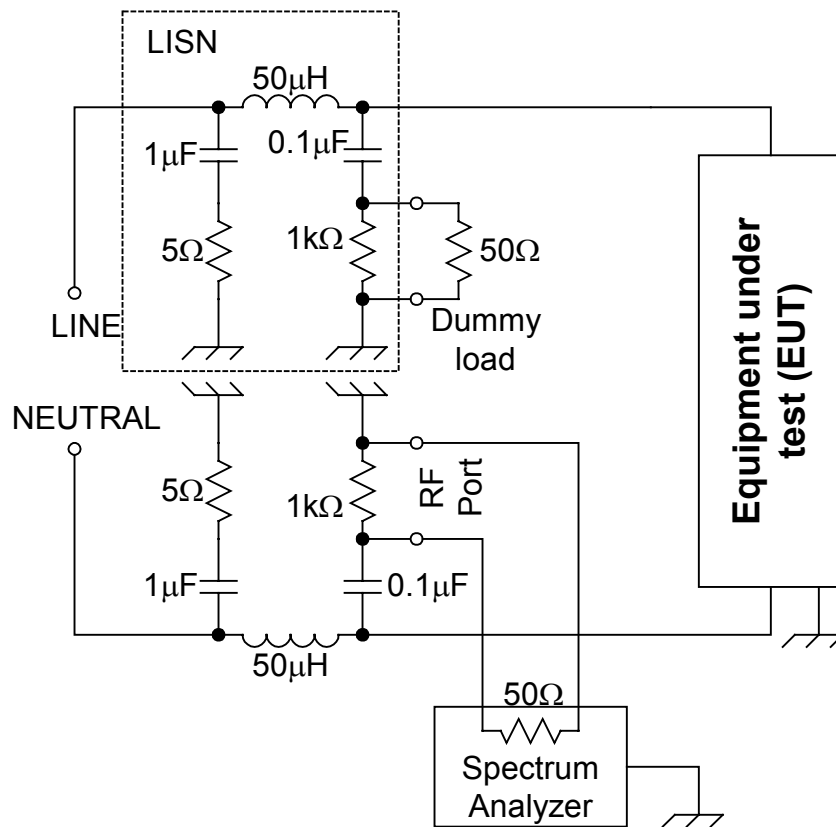


Fig. 2-16. Single-phase conducted EMI simulation setup.

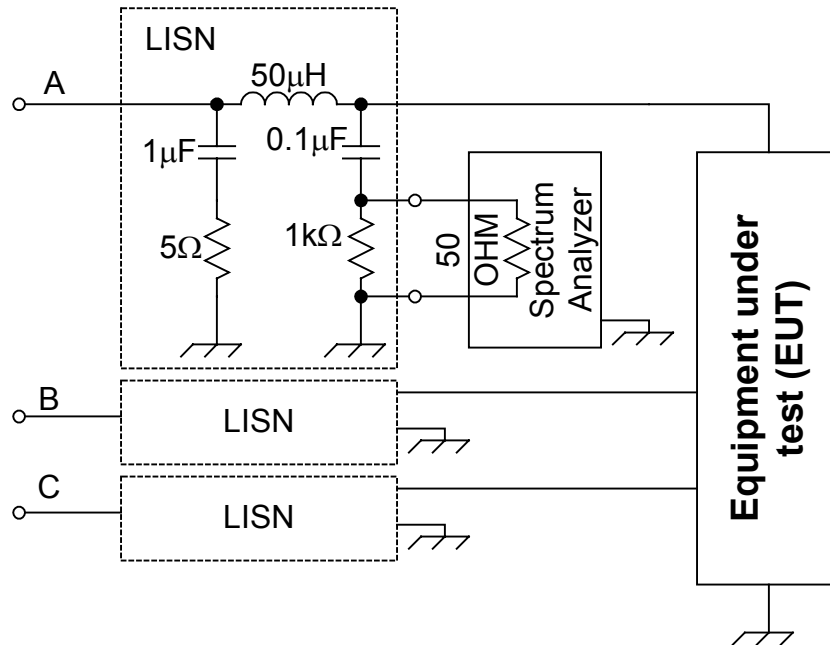


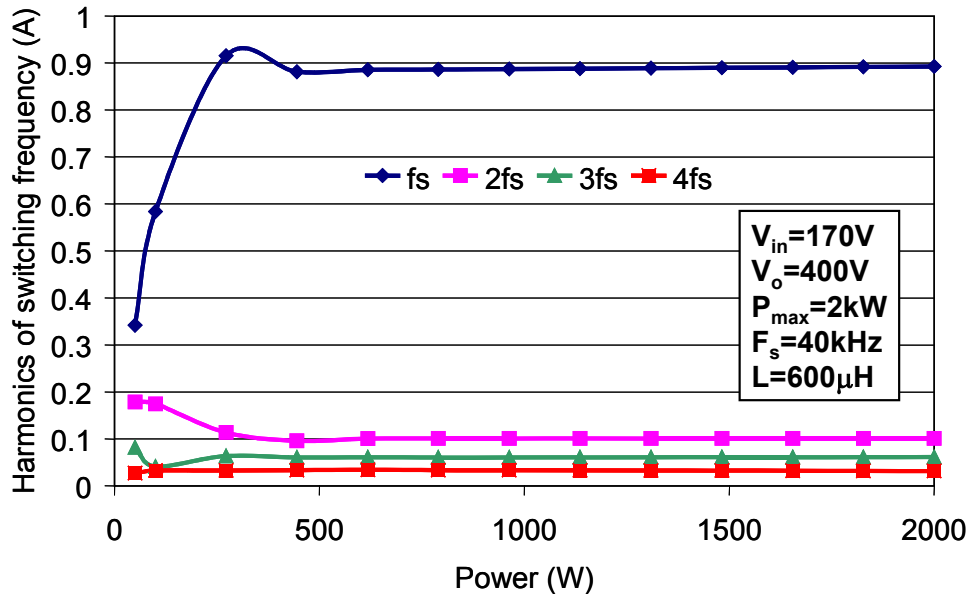
Fig. 2-17. Conducted EMI noise simulation setup for three-phase equipment.

2.7.2. *Worst-Case Ripple*

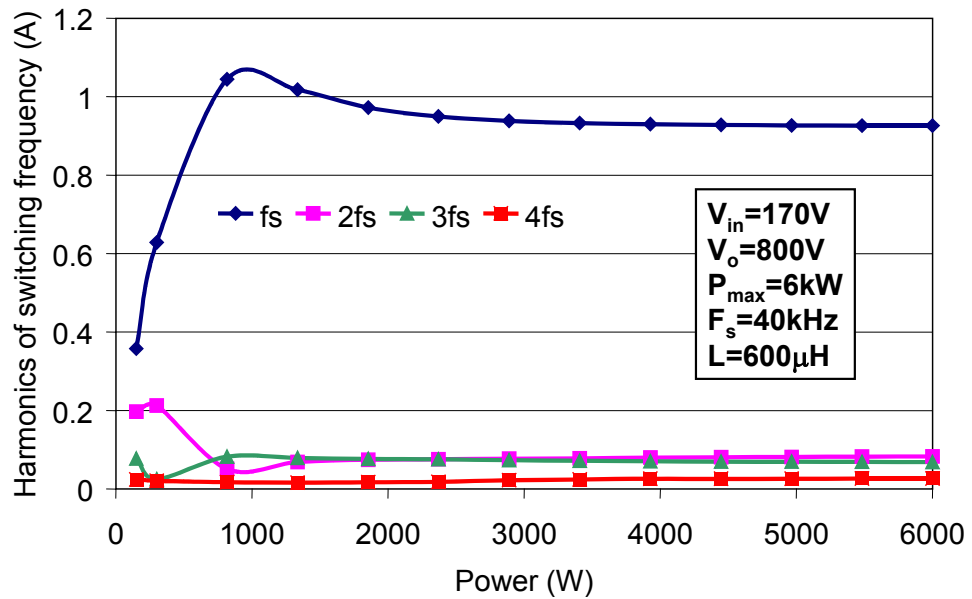
Identifying the worst-case input current ripple is rather important to assure that the DM input filter parameters are designed to attenuate the maximum noise. Fig. 2-18 illustrates how the most significant harmonics of the input current ripple change with the output power for both CCM boost (Fig. 2-18(a)) and VIENNA (Fig. 2-18(b)) rectifiers. As can be verified, both CCM rectifiers generate similar harmonics for similar converter parameters. These harmonics were obtained for a switching frequency of 40kHz, but the spectrum shape remains the same when different switching frequencies are used.

Fig. 2-19 illustrates the harmonics of the input current ripple for the following cases: (a) a single-unit non-interleaved DCM single-switch boost rectifier supplying 6kW and (b) a two-channel 6kW interleaved system. As can be seen, the non-interleaved DCM boost rectifier generates a

large harmonic content at the switching frequency, while the interleaved system eliminates the harmonics around f_s and other odd harmonics. Since both systems in Fig. 2-19 process the same power and use equivalent parameters, the even harmonics are identical in both cases.

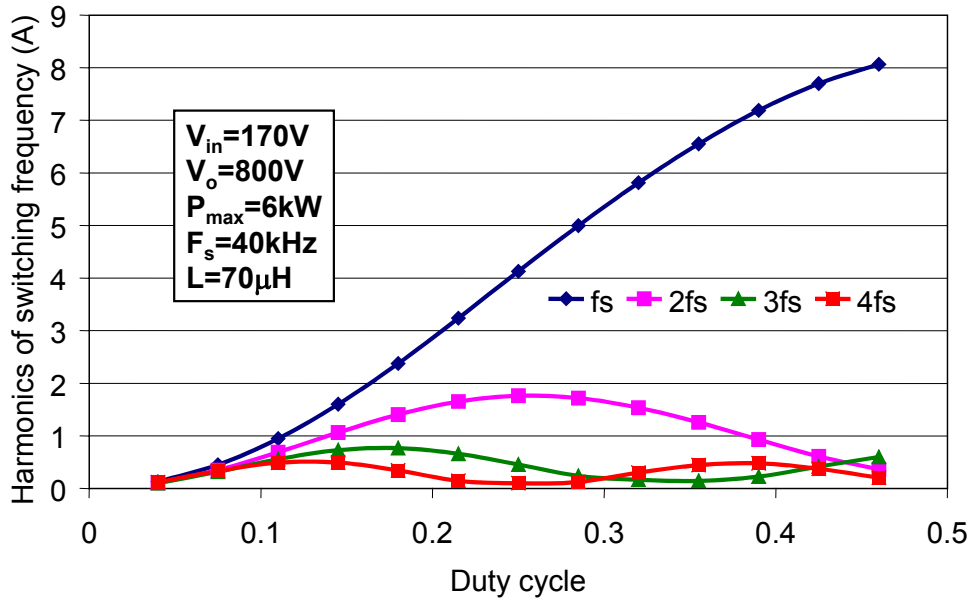


(a)

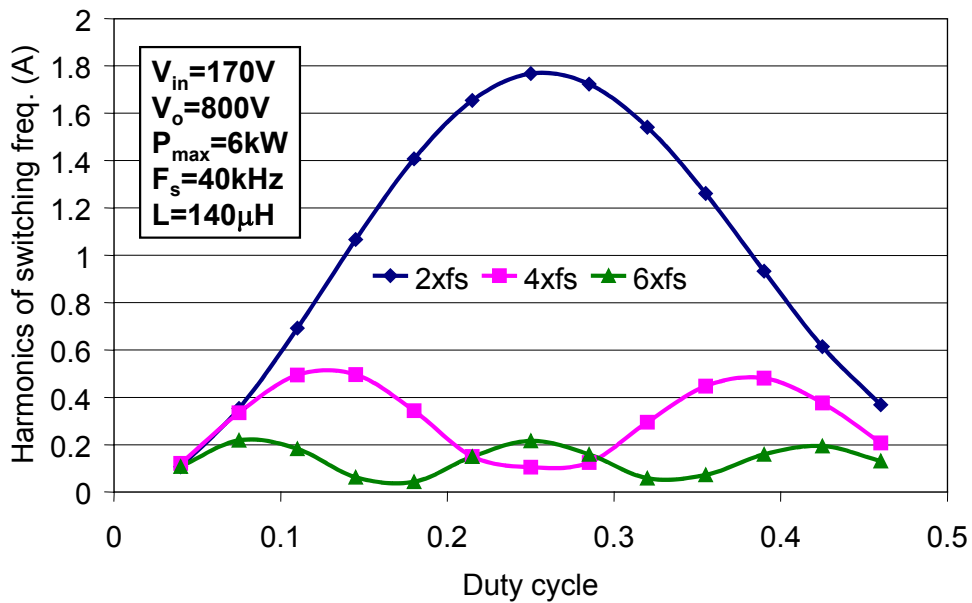


(b)

Fig. 2-18. Input current ripple harmonics: (a) single-phase CCM boost rectifier (2kW) and (b) VIENNA rectifier (6kW total power – 2kW per phase).



(a)



(b)

Fig. 2-19. Input current ripple harmonics: (a) one non-interleaved DCM boost rectifier (6kW), and (b) two-interleaved rectifiers (6kW).

2.7.3. Design Considerations

Fig. 2-15(a) shows the maximum noise profiles allowed by the VDE 0871 and CISPR 22 Class B standards (see page 56). The VDE is a difficult standard to comply with because it starts to limit

the noise at 10kHz, which means that the entire high-frequency spectrum generated by modern power electronics equipment must be considered when calculating the filter parameters. In the calculation of the DM input filter, it is assumed that the common-mode noise generated by the systems under consideration is neglected. This assumption allows the EMI standard profiles to be used to limit the emissions of DM noise [55]. Furthermore, the calculations hereafter consider average, instead of quasi-peak noise.

Table 2-6 illustrates for $f_s=40\text{kHz}$ the operating point at which the DM filter must be designed to attenuate the worst-case input current ripple. These operating points have been determined with the help of the curves illustrated in Fig. 2-18 and Fig. 2-19. For instance, consider the noise generated by the interleaved system, as shown in Fig. 2-19(b). If the DM input filter were designed to satisfy the VDE standard at a switching frequency of 40kHz, then one can conclude that the worst-case ripple would occur at $2xf_s$, since this frequency would be the first harmonic to be limited by VDE. More specifically, the worst-case ripple would occur at $2xf_s$ when $D=0.25$. Similarly, if the filter were designed according to CISPR, then the worst-case ripple would occur at $4xf_s=160\text{kHz}$ when $D=0.39$.

The comparison of the DM input filter size is provided for switching frequencies that vary from 40kHz to 200kHz. By considering such a range, it is possible to predict at what switching frequencies each of the cases under comparison is most effective in reducing the size of the input filter. Besides considering the size of the input filter, it is also important to take into account the size of the boost inductors required for each case.

Fig. 2-20(a) shows the boost inductance required by each case as a function of the switching frequency. For the interleaved system, the curve shown in Fig. 2-20(a) represents each

inductance required to implement the interleaved system. Because the inductance alone cannot be related to inductor size, the remaining information shown in Fig. 2-20 illustrates the core weight, winding and total weight for the boost inductors in each case under comparison.

Table 2-6. Identifying the DM filter design point (example: $f_s=40\text{kHz}$).

System	VDE 0871 Class B	CISPR 22 Class B
CCM boost	$V_{in}=170\text{V}$ and $P_o=2\text{kW}$ ³ $f_{att}=40\text{kHz}$	$V_{in}=170\text{V}$ and $P_o=2\text{kW}$ $f_{att}=160\text{kHz}(4xf_s)$
VIENNA	$V_{in}=170\text{V}$ and $P_o=6\text{kW}$ ⁴ $f_{att}=40\text{kHz}$	$V_{in}=170\text{V}$ and $P_o=6\text{kW}$ $f_{att}=160\text{kHz}(4xf_s)$
DCM non-interleaved	$V_{in}=170\text{V}$, $D=0.46$ and $P_o=6\text{kW}$ $f_{att}=40\text{kHz}$	$V_{in}=170\text{V}$, $D=0.39$ and $P_o=4.4\text{kW}$ $f_{att}=160\text{kHz}(4xf_s)$
Interleaved System	$V_{in}=170\text{V}$, $D=0.25$ and $P_o=1.89\text{kW}$ $f_{att}=80\text{kHz}(2xf_s)$	$V_{in}=170\text{V}$, $D=0.39$ and $P_o=4.4\text{kW}$ $f_{att}=160\text{kHz}(4xf_s)$

The inductor design procedure is given in Appendix I. The Kool M μ powder core material has been used in the design [58], while the temperature rise has been always limited to less than 55°C. Fig. 2-20(b) shows the core material weight needed to implement the boost inductors per phase (for the interleaved system, the weight shown refers to both boost inductors used per phase). Despite the lower inductance calculated for the DCM boost rectifiers, the amount of core is comparable to the CCM boost and VIENNA rectifiers because the core loss increases at high frequency in the DCM case. Fig. 2-20(c) shows the calculated amount of Cu needed to wind the inductors. The inductors for the CCM circuits require more Cu because the number of turns is

³ Although the highest noise occurs at $P_o \approx 300\text{W}$ (see Fig. 2-18(a)), the design of the DM input filter according to the VDE standard is done at full load for the CCM boost rectifier. The difference between the noises generated at 2kW and 300W is minimal and should not affect the comparison.

⁴ The same observation is valid for the VIENNA rectifier. Even though the highest noise occurs at $P_o \approx 900\text{W}$ (see Fig. 2-18(b)), the design of the DM input filter according to the VDE standard is done at full load for the VIENNA rectifier.

higher in order to provide large inductances. The combined core material and Cu weight is shown in Fig. 2-20(d), which illustrates that the total weight of the inductors used in the DCM rectifiers is lower than the weight of the inductors used in the CCM rectifiers.

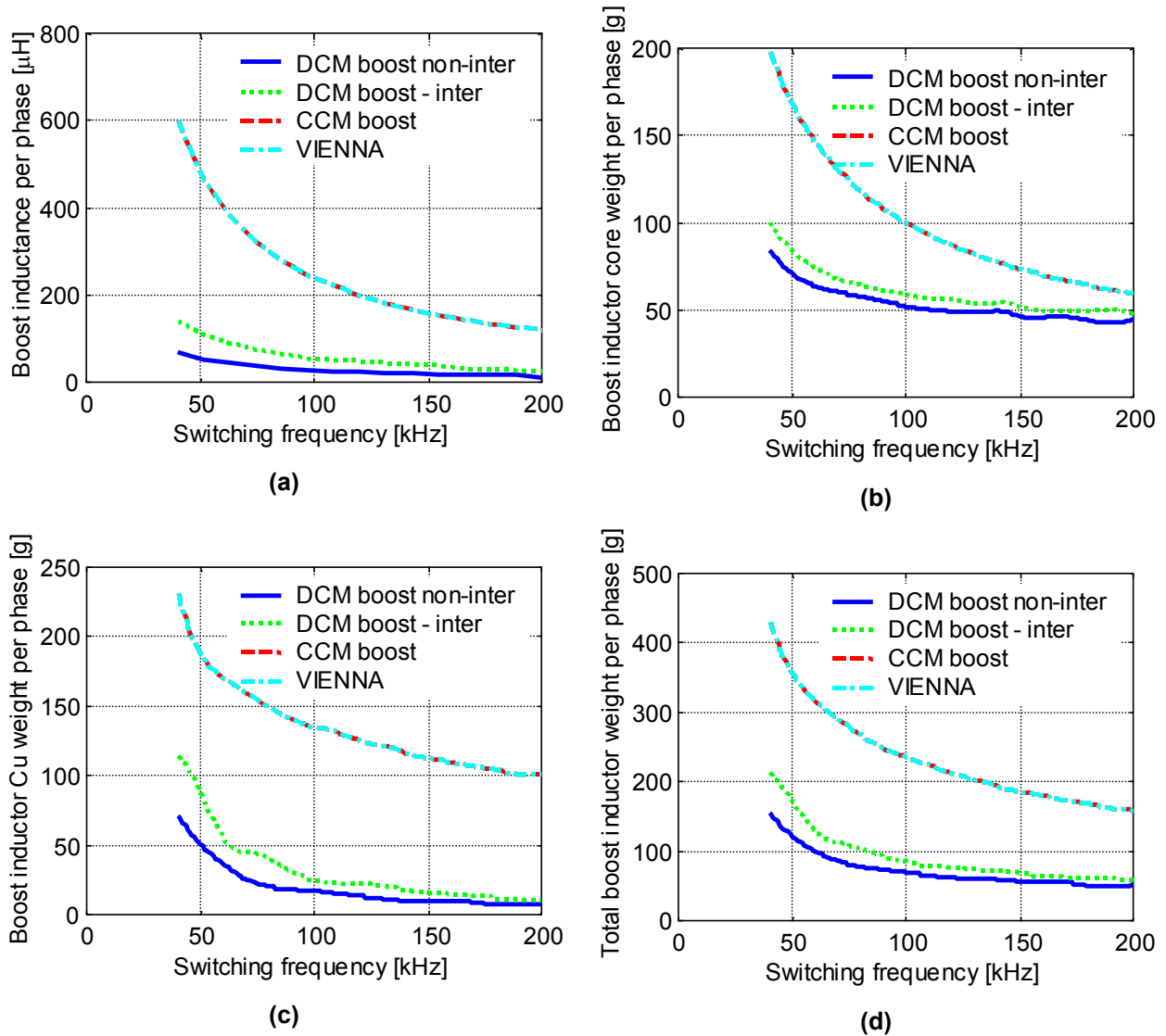


Fig. 2-20. Boost inductor design results: (a) boost inductance, (b) core weight, (c) Cu weight, and (d) combined core + Cu weight per phase.

2.7.4. DM Filter Parameters for the VDE 0871 Class B Standard

The determination of the filter parameters follows the steps described in Appendix II, while the total capacitance per phase for all cases under comparison can be calculated according to [56]:

$$(2-32) \quad C_{\max} = \frac{I_{pk-\min}}{2\pi f_r V_{pk-\text{high}}} \tan(a \cos(DF)),$$

where $I_{pk-\min}$ is the peak line current at light load (usually defined as 15% of the full power), $V_{pk-\text{high}}$ is the peak line-to-neutral input voltage at high line, and DF is the displacement factor at light load, which has been set to 0.95 throughout this dissertation.

The equivalent filter per phase used in the calculations is shown in Fig. 2-15(b) (see page 56). The results are presented in Fig. 2-21, which shows the inductances L_1 and L_3 , the filter core weight and the combined core plus Cu weight to implement the filter inductors. The inductance L_2 is not considered in the calculation because its size does not affect the overall filter, since L_2 is not in the main path of the input current. The low-frequency bypass inductor L_d is considered to be identical to L_1 , not only in terms of inductance value but also size, while the total capacitance determined from (2-32) is $3.8\mu\text{F}$ for all cases. The Kool M μ material is also used to calculate the weight of the filter inductors used in the converters under comparison [58].

The impact of the interleaving technique in reducing the filter size under the VDE standard is clear from Fig. 2-21(c). The non-interleaved DCM boost rectifier requires a huge amount of core material to implement the filter inductors in order to provide appropriate attenuation. On the other hand, the interleaved system requires even less filtering than the CCM boost and VIENNA rectifiers.

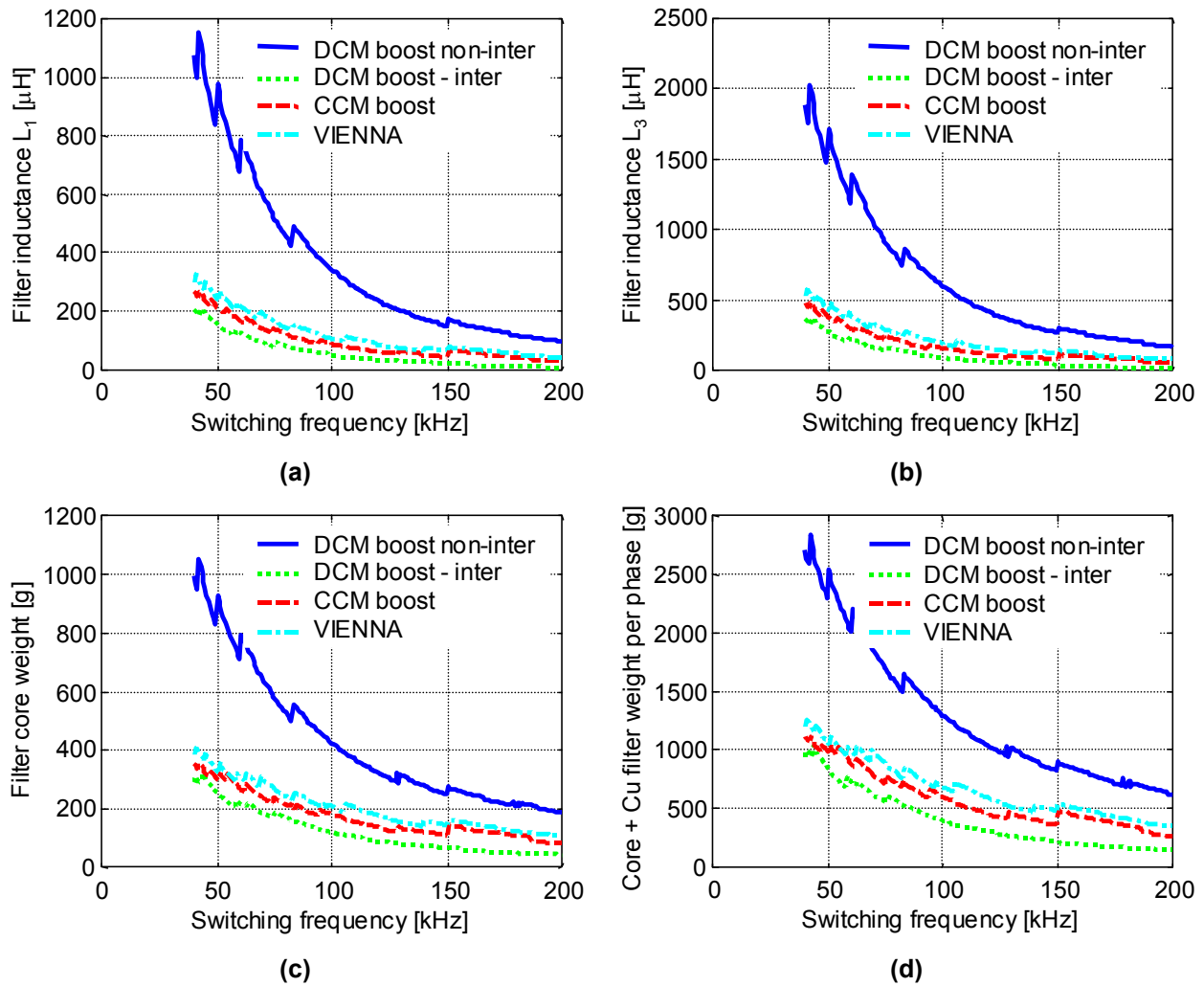


Fig. 2-21. Filter size for VDE 0871 Class B: (a) filter inductance L_1 , (b) filter inductance L_3 , (c) filter core weight to implement $L_d+L_1+L_3$ and (d) Core + Cu weight per phase required to implement $L_d+L_1+L_3$.

2.7.5. DM Filter Parameters for CISPR 22 Class B Standard

Although the interleaving technique was effective in reducing the size of the DM input filter for the VDE standard, it remains to be determined whether or not the same reduction occurs when the CISPR 22 is taken into account. To answer this inquiry, a similar evaluation was carried out to calculate the weight of the DM input filter using the CISPR 22 Class B standard.

The results are shown in Fig. 2-22, where the first observation made is that the amount of inductance per phase is drastically reduced in all cases as compared to the inductances calculated for the VDE standard. The second observation is that interleaving does not necessarily reduce the amount of filter inductance. As a matter of fact, for switching frequencies below 50kHz, the interleaved system is not even better than the non-interleaved DCM boost rectifier. In addition, below 50kHz the CCM boost and VIENNA rectifiers require a minimal amount of filter inductance per phase. The interleaving becomes more advantageous above a switching frequency of 150kHz. However, at that switching frequency, effective soft-switching techniques are required for proper operation.

Fig. 2-22(c) shows the amount of magnetic core material (Kool M μ powder core) needed to implement the filter inductors L_d , L_1 and L_3 for one phase, while Fig. 2-22(d) includes the Cu weight in the evaluation. As can be seen, the interleaved system is most advantageous at frequencies above 150kHz. The CCM and VIENNA rectifiers require smaller filters below 150kHz than any other DCM boost rectifier, with the best points for reducing the DM filter size defined at 50kHz, 70kHz and 150kHz. The interleaved system presents some advantage over the non-interleaved DCM boost rectifier for switching frequencies between 50kHz and 75kHz.

Although interleaving does not result in a reduced filtering requirement for the CISPR 22 standard, it is important to remember that the DCM rectifiers require smaller boost inductors than their CCM counterparts, as shown in Fig. 2-20(d). Therefore, combining the weight of filter and boost inductors per phase certainly changes the comparison results, as shown in Fig. 2-23. The combined filter with boost inductor magnetic core weights is shown in Fig. 2-23(a), while the incorporation of Cu into the evaluation is shown in Fig. 2-23(b). As can be seen, between

50kHz and 75kHz, the interleaved system is already competitive when compared to the CMM boost and VIENNA rectifiers. Above a switching frequency of 150kHz, the interleaved system is deemed the most effective in reducing the weight of boost and filter inductors.

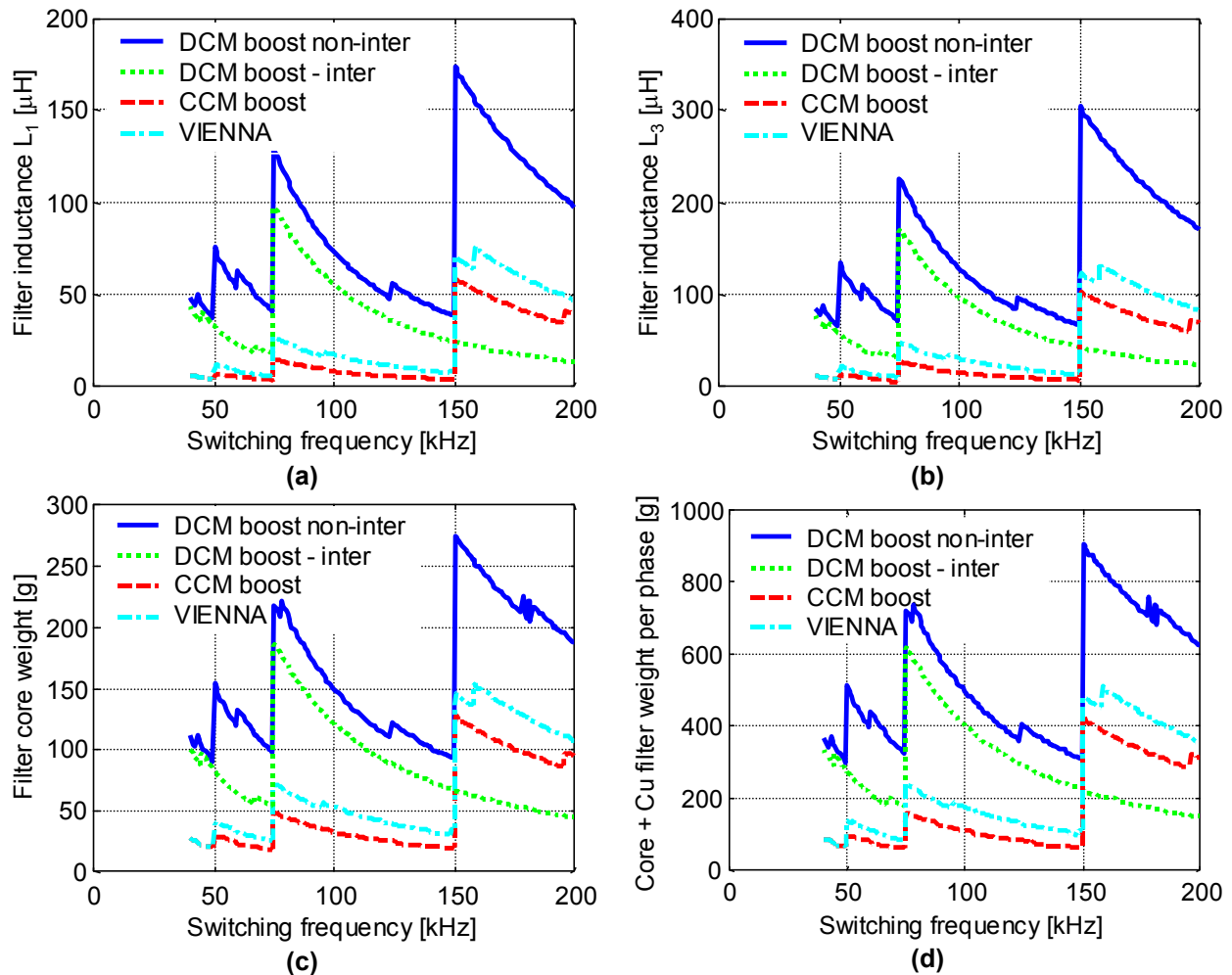


Fig. 2-22. Filter size for CISPR 22 Class B: (a) filter inductance L_1 , (b) filter inductance L_3 , (c) filter core weight to implement $L_d+L_1+L_3$, and (d) Core + Cu weight per phase required to implement $L_d+L_1+L_3$.

2.8. Two-Stage Front-End Converter Using the Interleaved Single-Switch DCM Boost Rectifier As the Front-End PFC

As discussed in chapter 1, a two-stage front-end converter consists of a PFC pre-regulator circuit followed by a DC/DC converter used to regulate the DC output voltage. In such a configuration,

the bus capacitor is placed between the two front-end converters. For practical applications, the intermediate bus capacitance must be large enough to decouple both the operation and the dynamics of the two power conversion stages. For this reason, each stage can be designed and optimized separately.

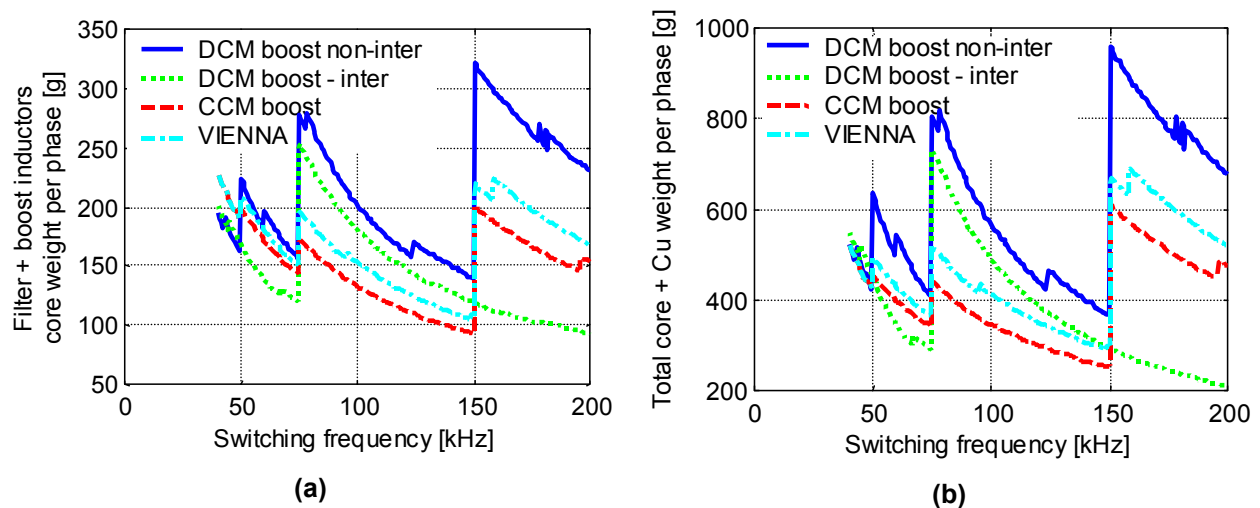


Fig. 2-23. (a) Combined filter and boost inductor core weight per phase and (b) total core + Cu weight needed to implement the boost and filter inductors per phase.

2.8.1. DC/DC Topology for 800V Bus Voltage Applications

In single-phase applications, the PFC circuit controls the intermediate bus voltage so that it stays at 400V, making the full-bridge converter shown in Fig. 2-24(a) the preferred topology for DC/DC power conversion. Since the bus voltage is regulated at 400V, the use of 500V MOSFETs in the DC/DC converter is feasible. Devices rated at 500V present very good R_{ds-on} characteristics, boosting up the efficiency of the entire system. The full-bridge converter is widely used in power electronics systems for applications above 1kW, and has an extensive list of performance improvements achieved along the years [59]-[61].

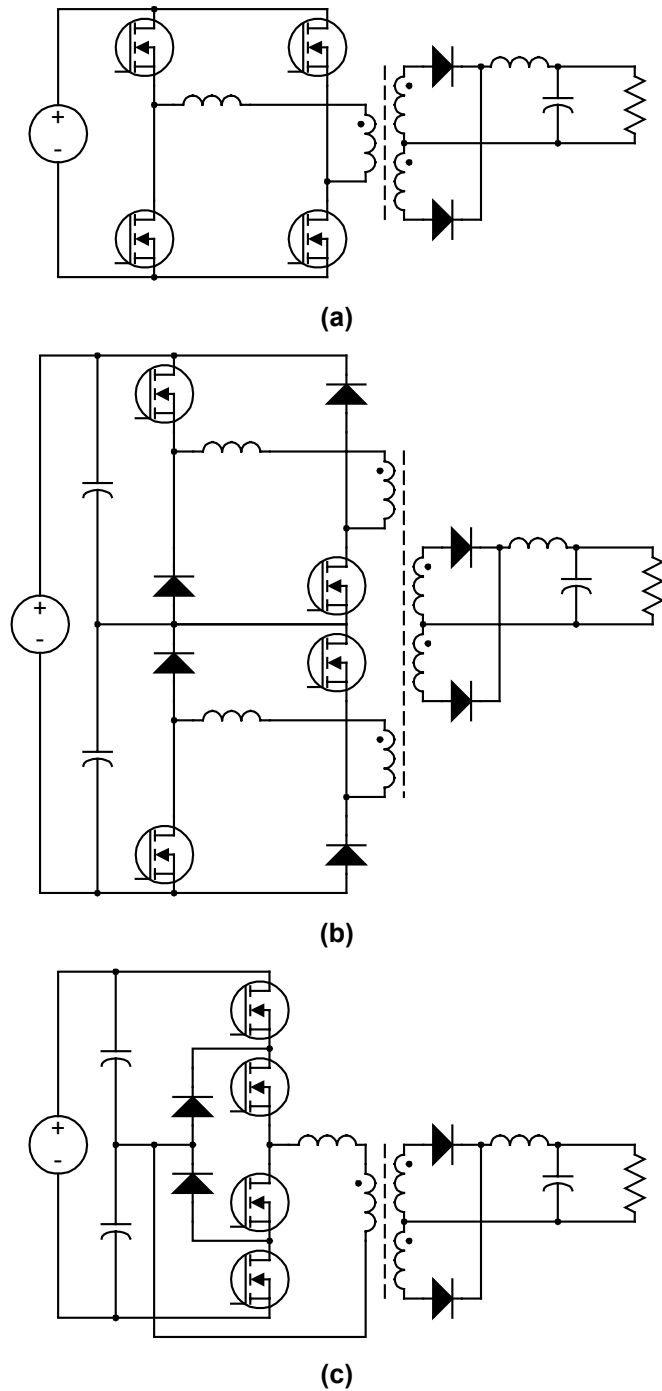


Fig. 2-24. DC/DC power conversion topologies: (a) full-bridge, (b) dual-bridge and (c) three-level.

In three-phase applications, however, if the nominal line-to-line input voltage is chosen to be 380V, the intermediate bus voltage is usually controlled to 800V by the PFC stage. Therefore, the DC/DC converter must handle the intermediate bus voltage stress, while still operating with

high efficiency and high power density. The choice of a full-bridge topology to be used for the DC/DC converter is not so clear in this type of three-phase application because the device voltage rating must be at least 1000V. For this voltage rating, power MOSFETs would not offer good R_{ds-on} characteristics, since they would increase the conduction loss in the circuit. On the other hand, if IGBTs were used in the DC/DC converter, the switching frequency would have to be lower to avoid high turn-off loss. Reducing the switching frequency would decrease the power density of the entire system, which is not desirable. Therefore, it is necessary to investigate different solutions for this type of high-voltage application. In fact, other topologies, such as the dual-bridge and the three-level DC/DC converters, are potential candidates [13]-[15]. The main advantage of these converters is that 500V devices can still be used to implement the circuit despite the bus voltage being 800V, as illustrated in Fig. 2-24(b) and Fig. 2-24(c).

To show the major differences between the efficiencies of the full-bridge and the three-level topologies, Fig. 2-25 shows a theoretical comparison between a three-level converter using 600V MOSFETs (APT60M75JVR, 600V/62A and $R_{ds-on}=0.075\Omega$) and a full-bridge converter using 1000V MOSFETs (APT10025JVR, 1000V/34A and $R_{ds-on}=0.25\Omega$). These devices represented the state-of-the-art power MOSFETs when the comparison was carried out in 2000. Conduction and switching losses have been taken into account in the power switches, while only conduction loss was considered in the output rectifiers. As can be seen, the three-level converter using 600V devices results in better efficiency. It is also important to mention that 600V devices present lower cost than their 1000V counterparts. Better efficiency and lower device cost justified the choice of the three-level converter for applications in which the intermediate bus voltage is 800V.

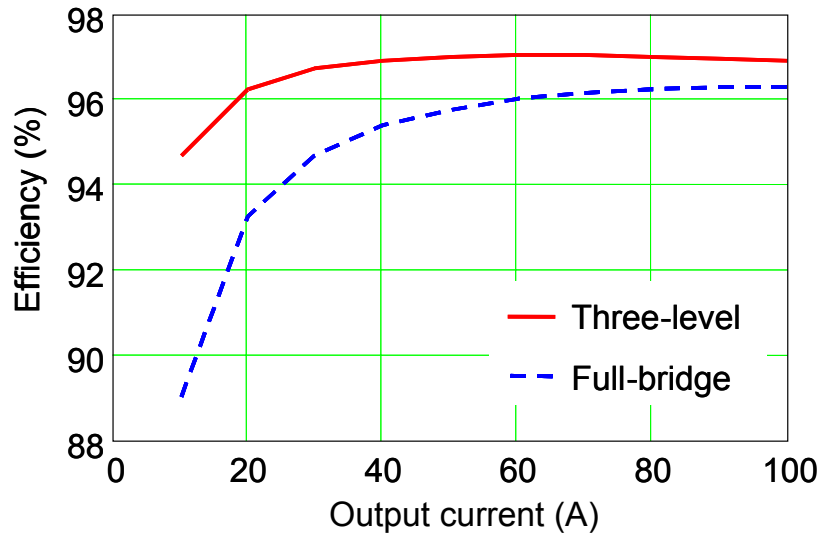


Fig. 2-25. Theoretical efficiency calculated for full-bridge and three-level converters.

Soft-switching techniques are necessary in order to improve the converter efficiency at higher switching frequencies. Purely ZVS converters rely on the energy stored in the resonant inductance placed in the primary side of the converter to achieve zero-voltage turn-on. A large resonant inductance increases the load range in which the power switches operate with zero-voltage turn-on, while increasing the circulating energy in the circuit [62]. In addition, the resonant inductance placed in the primary side of the DC/DC converter oscillates with the junction capacitance of the secondary-side rectifier, causing overshoot and requiring snubbers to damp the oscillations. These problems can be overcome when zero-voltage and zero-current switching (ZVZCS) techniques are used instead of the purely ZVS schemes. The ZVZCS techniques also reduce the circulating energy in the primary side of the transformer, providing zero-voltage turn-on for the outer switches of the three-level topology and zero-current turn-off for the inner switches, while drastically reducing the secondary-side parasitic ringing across the output rectifier diodes [63] [64]. To achieve ZVZCS operation, each switch in the three-level DC/DC converter operates with nearly 50% duty cycle. As shown in Fig. 2-26(a), it is also

necessary to connect a clamping capacitor in the primary side of the DC/DC converter to guarantee ZVS for the outer switches, as well as connect a secondary lossless circuit to reset the primary current during the freewheeling period in order to provide ZCS for the inner switches. Fig. 2-26(b) shows the primary voltage across the transformer (upper trace), the voltage across the output rectifier (middle trace) and the primary transformer current (lower trace). It can be observed that the primary current is reset to zero before the inner switches of the DC/DC converter are turned off, which characterizes a zero-current turn-off for the inner switches. The leakage inductance resonates with the capacitance of the lossless circuit placed in the secondary side, which is shown by the resonant peak seen in the primary current waveform. As can be seen, the voltage across the output rectifier of the three-level DC/DC converter does not present parasitic ringing. The parasitic ringing was eliminated in the waveform because the ZVZCS three-level converter does not need the resonant inductance to achieve soft switching for the inner switches. Therefore, the resonant inductance is simply the leakage inductance of the transformer, which is the reason for reducing the parasitic ringing across the secondary rectifiers.

Fig. 2-26(c) shows the drain-to-source voltage across the upper switch of the three-level DC/DC converter and its gate signal. The voltage across the switch decreases to zero before the gate signal is applied, which characterizes a zero-voltage turn-on for the outer switches of the three-level DC/DC converter. As can be verified, the switches in the three-level DC/DC converter support half of the total bus voltage. This allows the use of 600V MOSFETs with low R_{ds-on} in the implementation, or even 500V MOSFETs if the voltage margin is acceptable.

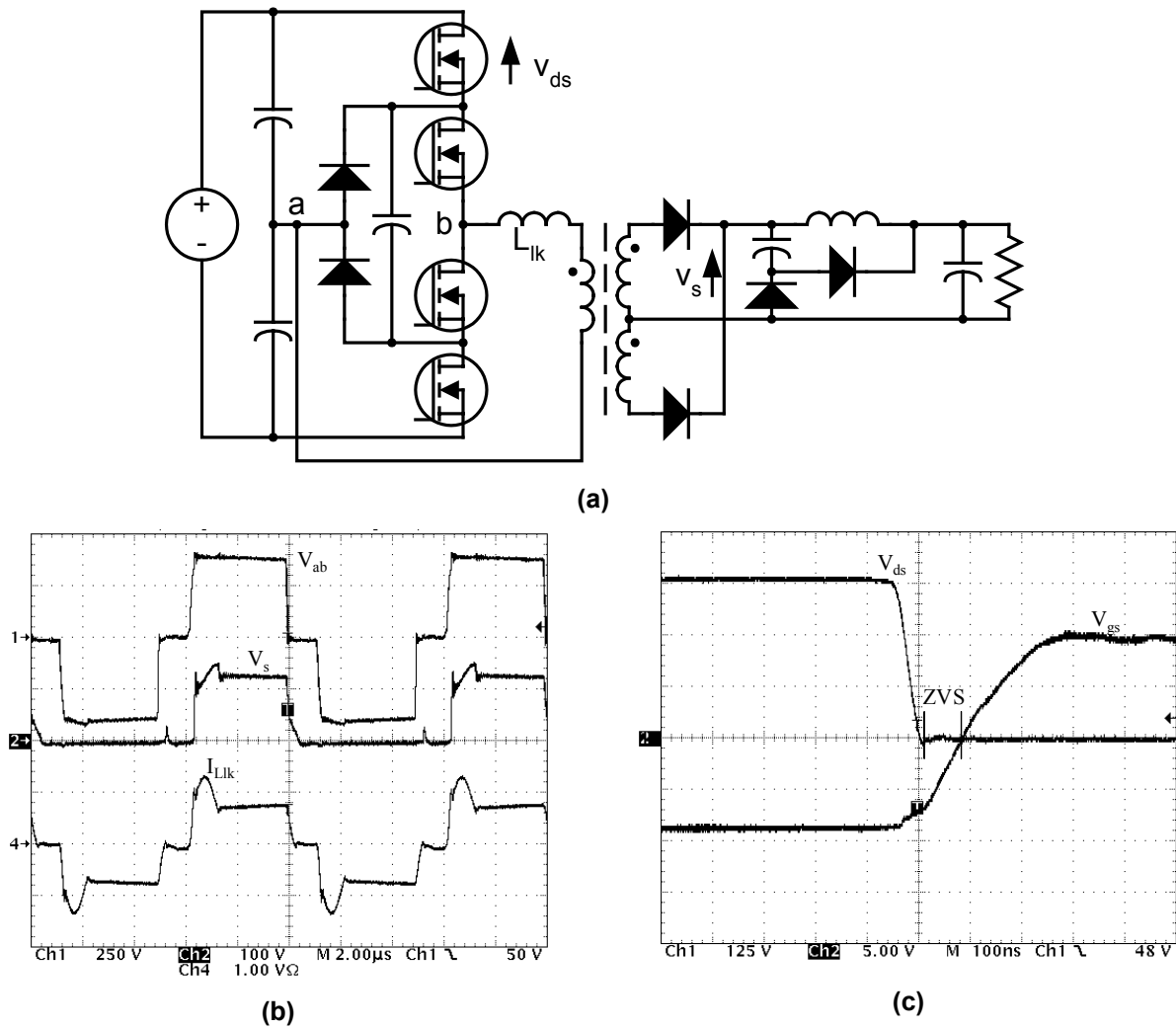


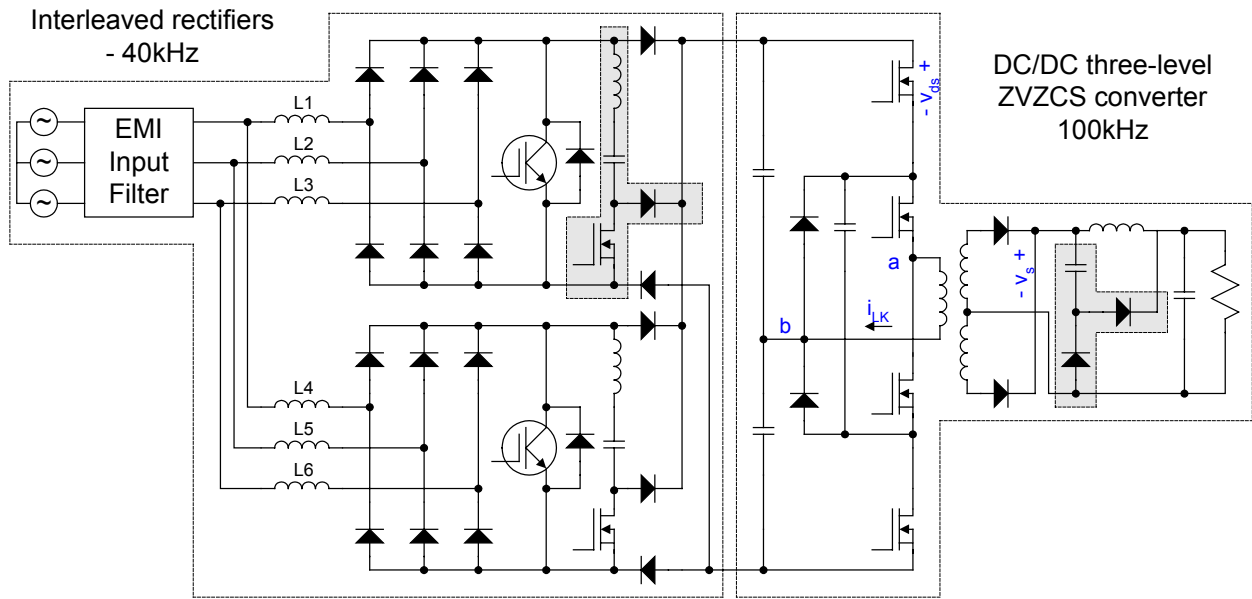
Fig. 2-26. (a) Three-level ZVZCS DC/DC converter used in the implementation of the two-stage front-end converter, (b) experimental results for v_{ab} , v_s and i_{Llk} (20A/div) at $P_o=5kW$, $V_{bus}=800V$, $V_{out}=52V$ and $f_s=100kHz$, and (c) ZVS transition for the outer switches.

2.8.2. Interfacing PFC and DC/DC Converters

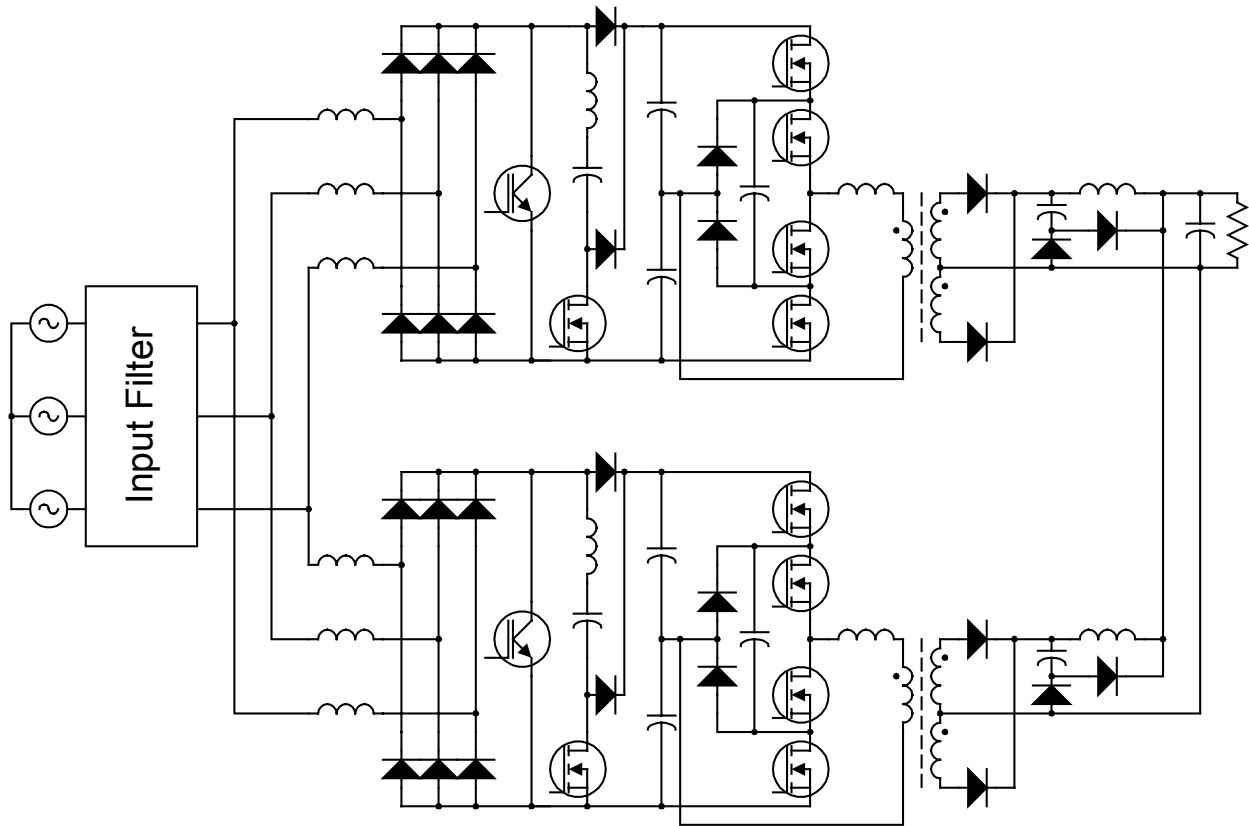
Fig. 2-27 shows two possible methods for realizing a front-end converter using interleaved DCM boost rectifiers and three-level DC/DC converters. In the first option, shown in Fig. 2-27(a), the DCM boost rectifiers are connected to the same bus voltage, while one three-level DC/DC converter is used to process the total output power. The second option, shown in Fig. 2-27(b), uses two individual channels to process the power. The main difference between the two

approaches is that in the second case, current sharing is still an issue and must be achieved in the output side of the three-level DC/DC converters, while in the first case no current sharing is needed because the boost rectifiers are connected together and they operate as current sources (see results in Fig. 2-12(a)). Evidently, the tolerance in the value of the boost inductances of the first option will dictate the level of current sharing achieved by connecting the DCM boost rectifiers to the same bus voltage. However, well-defined manufacturing procedures should guarantee that the inductance values are within a 10% tolerance, which should be sufficient to guarantee current sharing between the two DCM boost rectifiers connected to the same bus voltage.

Although the system shown in Fig. 2-27(a) is simpler and does not present current sharing issues, its counterpart shown in Fig. 2-27(b), using two three-level DC/DC converters, presents a higher level of modularity. Nevertheless, the DPS front-end converter was implemented using the first approach, shown in Fig. 2-27(a), whose main components are described in Table 2-7 for the 6kW application. For this particular example, the PFC stage was implemented at 40kHz of switching frequency using a ZCT circuit to provide zero-current turn-off for the main IGBT, while the three-level DC/DC converter was operated at 100kHz. Fig. 2-28 shows the individual converter and the overall system efficiencies at full load as a function of the line-to-neutral input voltage variation. The efficiency of the PFC stage changes linearly with the variation of the line-to-neutral voltage, while the efficiency of the three-level DC/DC converter remains constant over the entire input voltage variation. This is in agreement with the fact that the intermediate bus voltage is regulated by the PFC stage. The maximum overall efficiency is achieved at high-line input voltage, while the overall efficiency at 220V line-to-neutral input voltage is 90.8%.



(a)



(b)

Fig. 2-27. Front-end converters using interleaved DCM boost rectifiers: (a) common intermediate bus voltage, and (b) using two DC/DC converters.

Table 2-7. System parameters and components designed for 6kW application.

PFC Stage		DC/DC Stage	
Component	Parameter/Type	Component	Parameter/Type
Boost Inductance	140 μ H-E55/21	Switches	APT 60M90JN
Input Bridge Rectifiers	DSEI 30-10A	Clamping Capacitor	4 μ F/630V (polypropylene)
Switch	IXSN35N1200U1	Clamping Diodes	BYV34-500
Auxiliary Switch	IXTN15N100	Transformer	E67/27, 12/3/3turns, 1.2 μ H of leakage inductance
Resonant Series Inductance	5.7 μ H-E21	Output Rectifiers	HFA 140MD60C
Resonant Series Capacitance	40nF/630V	Lossless Capacitor	220nF
Boost Diode	DSEI 30-10A	Lossless Diodes	DSE 160-05A
ZCT Diode	DSEI 30-10A	Output Inductor	16 μ H-E55/21

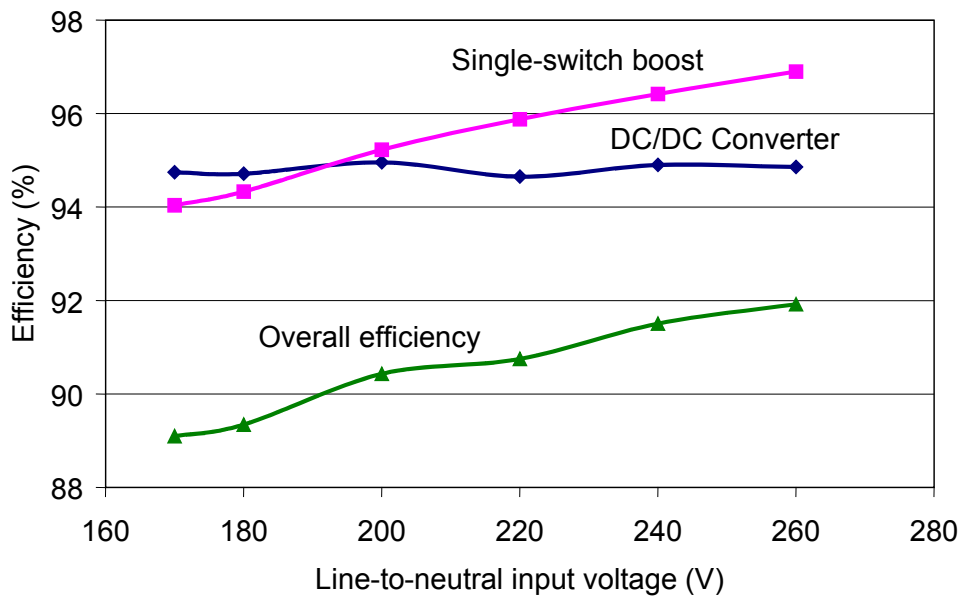


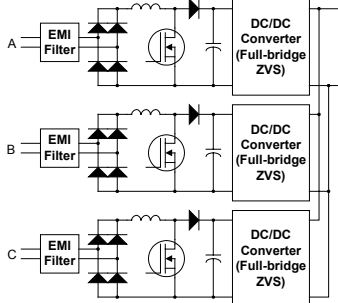
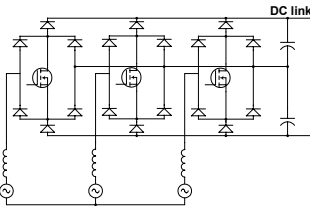
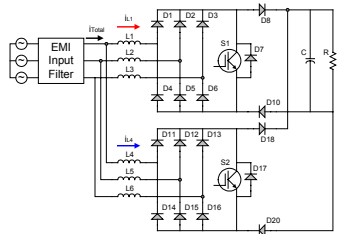
Fig. 2-28. System efficiency at 6kW, including EMI filter.

2.9. Benchmarking

As mentioned in chapter 1, the circuits described in this work are benchmarked against the CCM and VIENNA rectifier. Table 2-8 illustrates the comparison between the benchmark circuits and the single-switch DCM boost rectifier. The data marked up in blue represent advantages with respect to benchmark circuits, while red fonts represent disadvantages. From Table 2-8, one

concludes that the following points must be improved: switch voltage stress, THD, and efficiency.

Table 2-8. Benchmarking the single-switch DCM boost rectifier ($V_{in}=220V$ LN).

Topology	CCM Boost Rectifiers	VIENNA Rectifier	Interleaved Single-Switch DCM Boost Rectifiers
Feature			
Total power (kW)	6	6	6
Switches	3	3	2
Line freq. diodes	12	12	-
Fast diodes	3	6	16
Bus voltage (V)	400	800	800
Switch voltage (V)	400	400	800
RMS/AVG SW current (A)	5.5/3.2	5.5/3.2	4.9/2.3
AVG diode current			
Line freq. Diodes (A)	4.1	4.1	-
Fast diodes (A)	5	2.5	4.1 (input rec.) – 3.75 (output)
Output cap RMS current (A)	5.5	5.6	4.75
THD (%)	-	-	12.7
THD with harmonic injection	-	-	10.8
Efficiency (%) at 40kHz	98 (simulation)	98.2 (simulation)	95.8
Power under two-phase operation (kW)	4	4	3.4
Active current control	Yes	Yes	No
Sensing effort	Medium	High	Low
Control complexity	High	High	Low

2.10. Conclusion

This chapter explored and described the pros and cons of using the single-switch DCM boost rectifier as a PFC stage for applications in DPSs. Detailed analyses and simplified design guidelines were presented. The harmonic injection method demonstrated improvements in the quality of the currents drained from the power source. As a benefit of the harmonic injection technique, it is possible to extract more power from the DCM boost rectifier. For a bus voltage of 800V and an input phase voltage of 220V, the harmonic injection enables the extraction of 8kW from the single-switch DCM boost rectifier, as opposed to 6kW when no harmonic injection is used for the same input and output voltages.

As demonstrated throughout this chapter, interleaving DCM boost rectifiers provides high-frequency input current ripple cancellation. As a result of reducing the amplitude of the input current ripple, a reduction in filter size was demonstrated when the VDE 0871 standard was used to design the DM input filter. A comparison between the interleaved system, the non-interleaved DCM boost rectifier, and two benchmark circuits (CCM boost and VIENNA rectifiers) showed that interleaving is a very effective method for reducing the size of the DM input filter. The reduction in filter size was achieved because the VDE standard starts at 10kHz, requiring the entire spectrum to be attenuated.

On the other hand, when compared with the benchmark circuits, a reduction in filter size was not achieved. In fact, in terms of the weight of the magnetic cores needed to implement the filter inductors, both the non-interleaved DCM boost rectifier and the interleaved system yielded similar sizes below 50kHz of switching frequency. The interleaved system becomes more advantageous above 150kHz, but below this frequency the CCM boost and VIENNA rectifiers

required the least amount of filter inductors to provide appropriate attenuation. For the interleaved system to show some advantages under CIPSR 22, the size of the boost inductors must be included in the comparison. In that case, for switching frequency of 50kHz to 75kHz, the combined weight of the boost and filter inductors for the interleaved system becomes comparable to both the CCM boost and the VIENNA rectifiers. Above 150kHz, the interleaved system is deemed the most effective in reducing the size of the DM input filter.

Current sharing between the interleaved rectifiers can be easily achieved because the DCM boost rectifier operates as a current source. The accuracy level in the current sharing depends upon the difference between the inductances connected to the same phase. A tolerance of $\pm 10\%$ in the boost inductances would be accurate enough to guarantee good current sharing between the interleaved DCM boost rectifiers. To maintain input current ripple cancellation, it must be assured that there will be no phase-shift error in the gate signals of the interleaved rectifiers. As demonstrated, a phase-shift error of $\pm 10\%$ in the gate signals of the two interleaved rectifiers is sufficient to create a DM noise around the switching frequency, which is comparable to the noise at $2xf_s$.

A two-stage front-end converter for 6kW applications, based on the interleaved system connected in series with a three-level DC/DC converter, was tested. The system achieved an overall efficiency of 90.8%, which included the losses in the DM input filter. Despite the simplicity and excellent overall efficiency of the solution discussed in this chapter, there are still two drawbacks to overcome: the voltage stress across the switch of the PFC circuit and the reduction of the THD to below 10%.

3. Two-Switch Three-Level DCM Boost Rectifier

3.1. Introduction

Up to this point, three major methods for obtaining high-power front-end converters with PFC function were discussed: (1) the connection of single-phase modules to the three-phase system in order to achieve the required output power level [9]-[11], (2) the VIENNA rectifier [18], and (3) the single-switch DCM three-phase boost topology [42], including interleaved DCM boost rectifiers [51]. In the last approach, the boost inductors operate in DCM to achieve automatic input current shaping. The harmonic injection method was used in the single-switch DCM boost rectifier to increase the output power level while still meeting the IEC 61000-3-2 standard without increasing the output voltage beyond 800V [47]. Despite the improvements made in the operation of the single-switch DCM boost rectifier to avoid increasing the bus voltage beyond practical levels, the use of power MOSFETs with low on-resistance is not yet possible. To overcome this problem, this chapter presents a two-switch boost rectifier implemented in a three-level topology used to reduce the voltage stress applied across each switch. As a result of the reduced voltage, low on-resistance MOSFETs can be used in the power stage.

This chapter explores the main features of the two-switch three-level boost rectifier operated in DCM. The main contributions are reduced voltage stress, improved efficiency and reduced THD. Control strategies and design guidelines are provided throughout the text. The interleaving technique is also used to cancel the high-frequency input current ripple. The discussion is supported by simulation and experimental results obtained from a 6.3kW prototype.

3.2. Circuit Description

A similar version of the topology discussed hereafter, using variable-frequency control, has been previously presented [65]. The two-switch three-phase rectifier is shown in Fig. 3-1. The three-level structure is comprised of the switches S_1 and S_2 and diodes D_1 and D_2 . The capacitors C_1 and C_2 share the total bus voltage. The AC capacitors C_a , C_b , and C_c eliminate the neutral point connection of the power system, thus preventing any zero-sequence-order harmonic (3rd, 9th, 15th, etc...) from circulating in the input lines. The advantage of the three-level structure is that the voltage applied across the power switches is half of the total bus voltage, which enables the use of devices with lower voltage ratings.

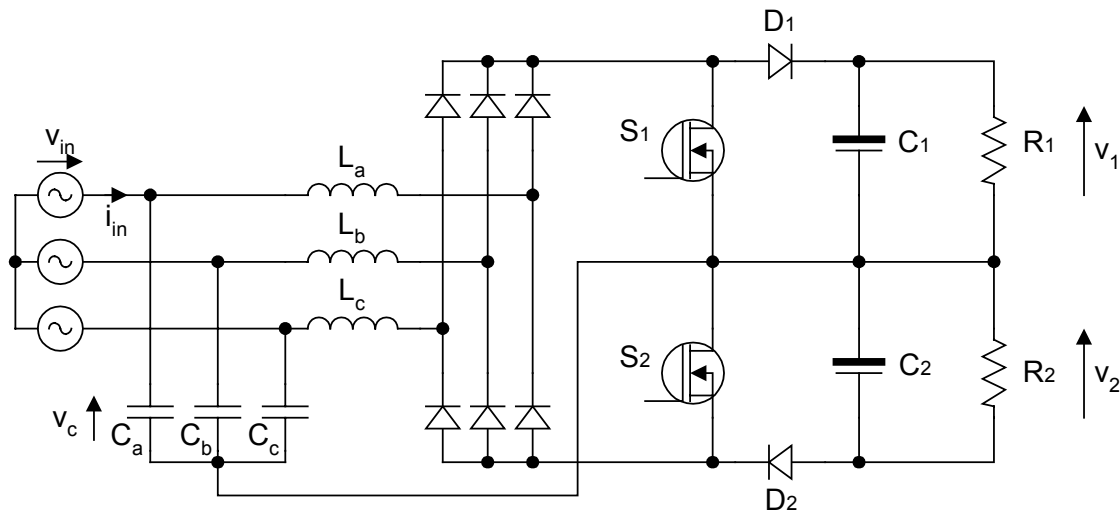


Fig. 3-1. Two-switch three-level PFC circuit.

Fig. 3-2 shows the operating stages of the two-switch three-level boost rectifier, while Fig. 3-3 illustrates the boost inductor current waveforms. To simplify the explanation, Fig. 3-2 neglects the AC capacitors. During one operating cycle, the switches S_1 and S_2 are simultaneously turned on to store energy in the input inductors (first stage). When the switches are turned off, the boost

inductors are fully reset by the difference between half of the bus voltage and the input voltage connected across the same phase of the boost inductor (second, third and fourth stages). In the fifth stage, which is not shown in Fig. 3-2, the output load is supplied by the energy stored in the bus capacitors.

3.3. Control Strategy and Voltage Balance Across the Bus Capacitors

Fig. 3-1 also shows a possible way to connect the output load to the rectifier. Instead of connecting a single load across the positive and negative DC rails, the load can be split between the output capacitors. Although this approach to connecting the output load is possible, if the converter is not properly controlled, any difference between the DC currents circulating through the split output loads results in an offset in the voltages across the AC capacitors, as well as in an imbalance of the voltages across C_1 and C_2 . Fortunately, this voltage imbalance across the bus capacitors can be somewhat compensated for by properly controlling S_1 and S_2 .

One possible scheme for controlling the voltage imbalance across C_1 and C_2 is presented in Fig. 3-4(a). As can be seen, S_1 is used to control the voltage across C_2 , whereas S_2 is used to control the voltage across C_1 . Both voltage controllers in Fig. 3-4(a) use the same voltage reference, which is $V_{bus}/2$.

Fig. 3-4(b) shows the simulation results obtained from a circuit that supplies a total power of 6kW at 170V line-to-neutral input voltage. The capacitance C_1 was set to 400 μ F and C_2 to 500 μ F, while the equivalent resistor R_1 draws 3.3kW from the rectifier and R_2 2.7kW. The control objective is to regulate the average voltages across C_1 and C_2 to 400V.

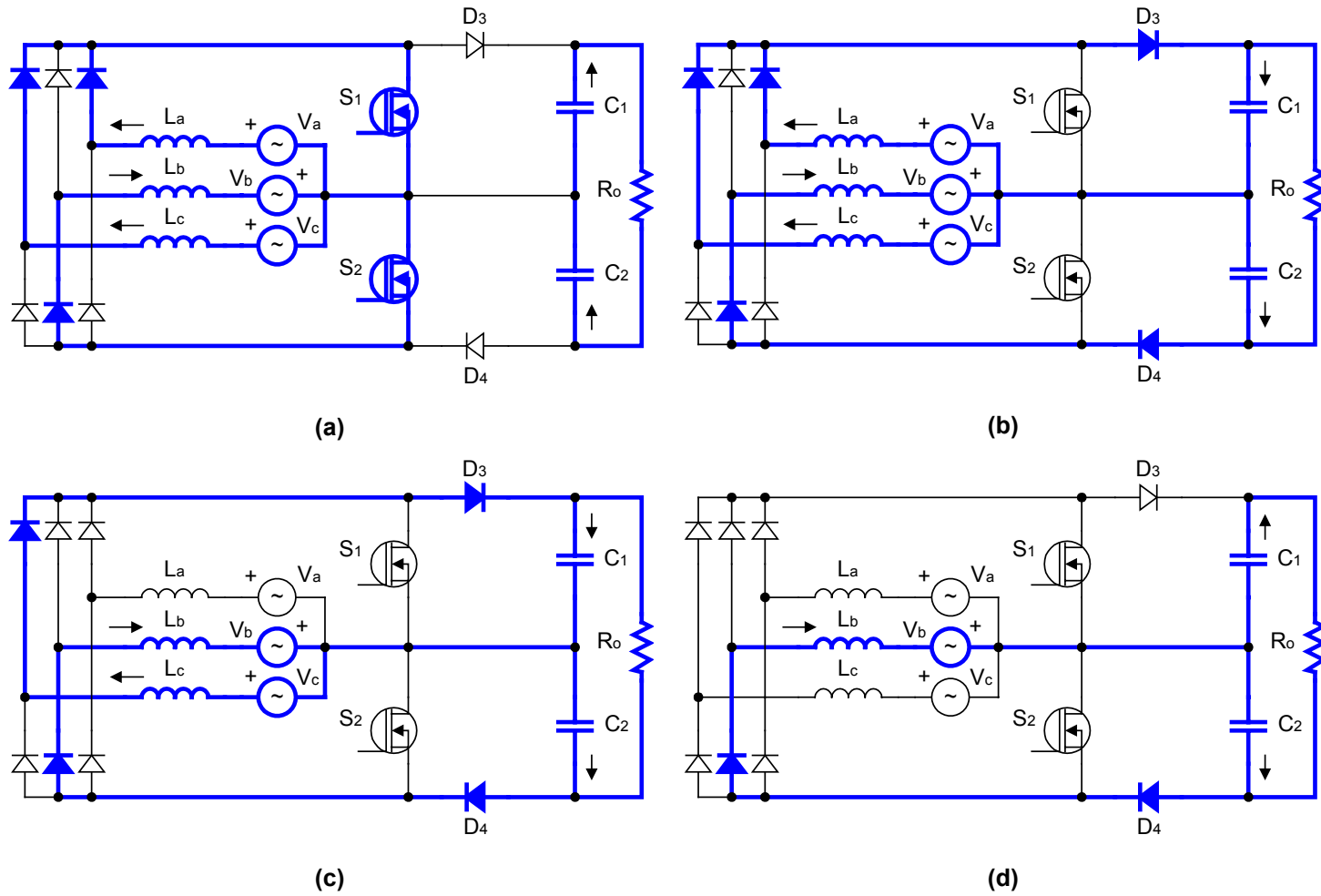


Fig. 3-2. Operating stages: (a) first stage (t_0, t_1), (b) second stage (t_1, t_2), (c) third stage (t_2, t_3), and (d) fourth stage (t_3, t_4).

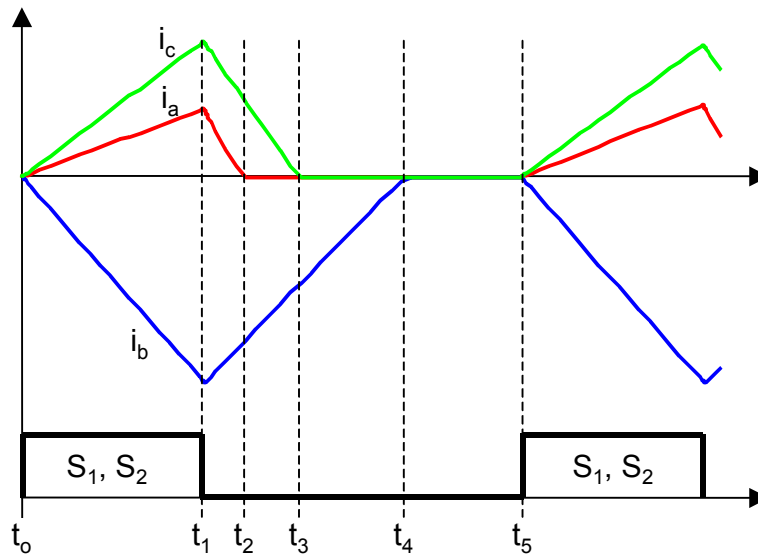


Fig. 3-3. Boost inductor current waveforms.

As can be verified in Fig. 3-4(b), the voltages across C_1 and C_2 are controlled to the targeted value, despite the imbalance in the split load and the mismatch between C_1 and C_2 . It is important to mention, however, that there is no means of regulating both voltages under severe load imbalance. For instance, suppose that R_2 is suddenly disconnected from the rectifier. In this case, the control signal that generates the duty cycle for S_1 is driven to zero. However, S_2 is still able to control the voltage across C_1 to 400V. Therefore, there is still current flowing through capacitor C_2 during the turn-off stage of S_2 . Since R_2 has been disconnected, it is no longer possible to assure the charge balance in C_2 , and the converter will not operate properly. Consequently, under a situation of extreme imbalance, such as the disconnection of one of the output loads, the rectifier must be shut down.

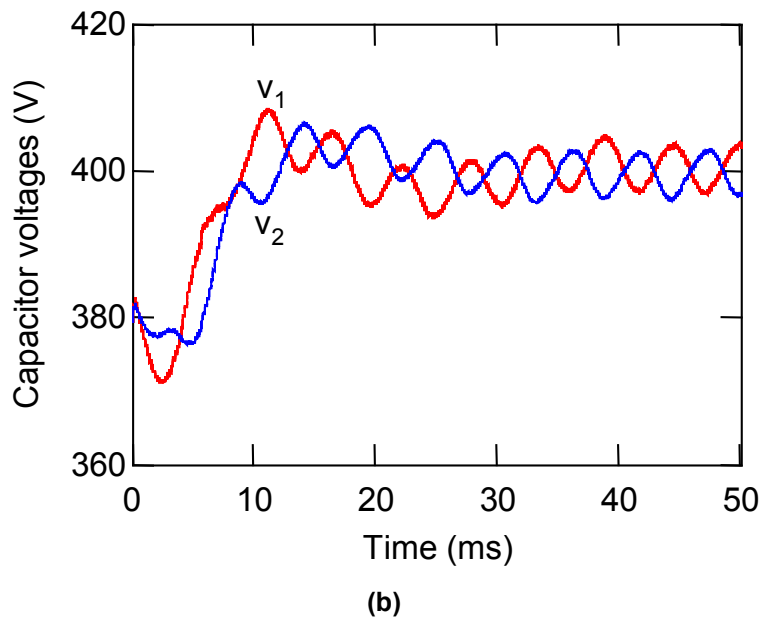
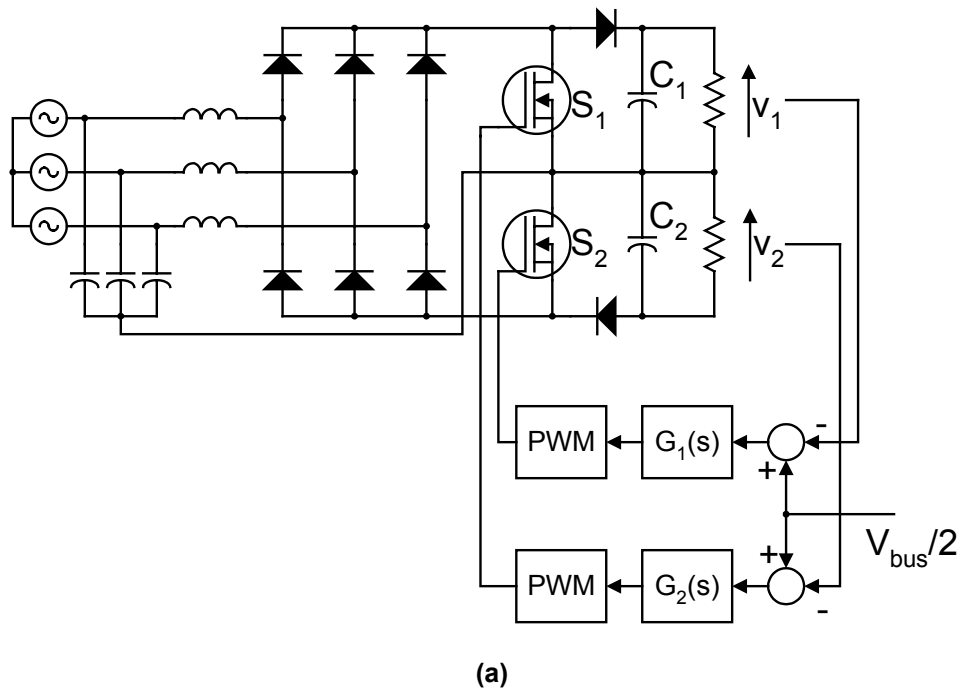


Fig. 3-4. Control of voltages across C_1 and C_2 : (a) control scheme and (b) simulation results.

The flexibility of using S_1 to control v_2 and S_2 to control v_1 enables the use of the two-switch three-level DCM boost rectifier, as illustrated in Fig. 3-5(a). Since the voltages across C_1 and C_2 can be individually controlled, conventional DC/DC converters usually designed to operate from

a 400V bus can be connected across the output capacitors. In another possibility shown in Fig. 3-5(b), the two-switch boost rectifier supplies power to a three-level DC/DC converter. Any duty cycle mismatch in the switches of the three-level DC/DC converter causes a voltage imbalance across C_1 and C_2 . This voltage imbalance, however, can be mitigated by the modulation scheme described in Fig. 3-4.

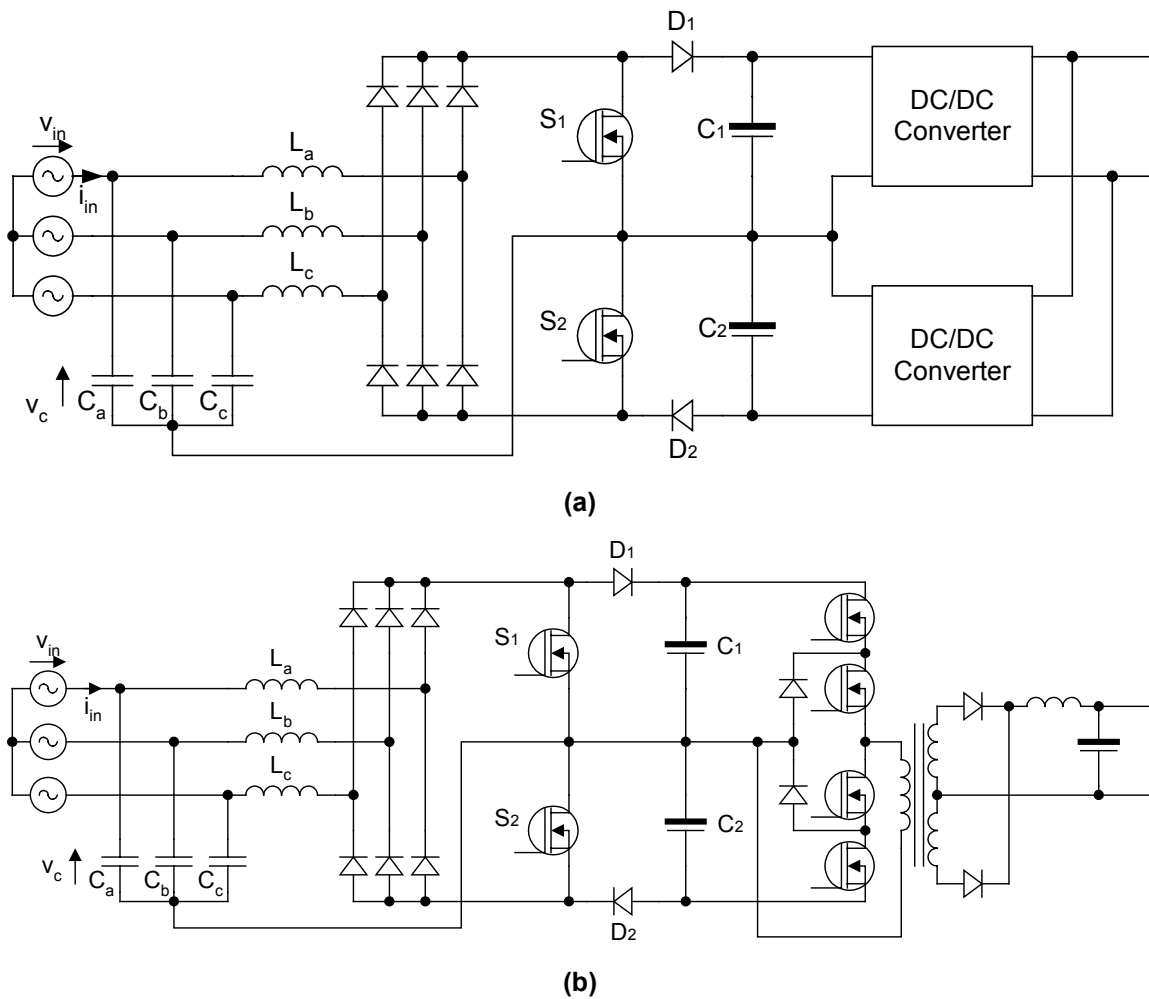


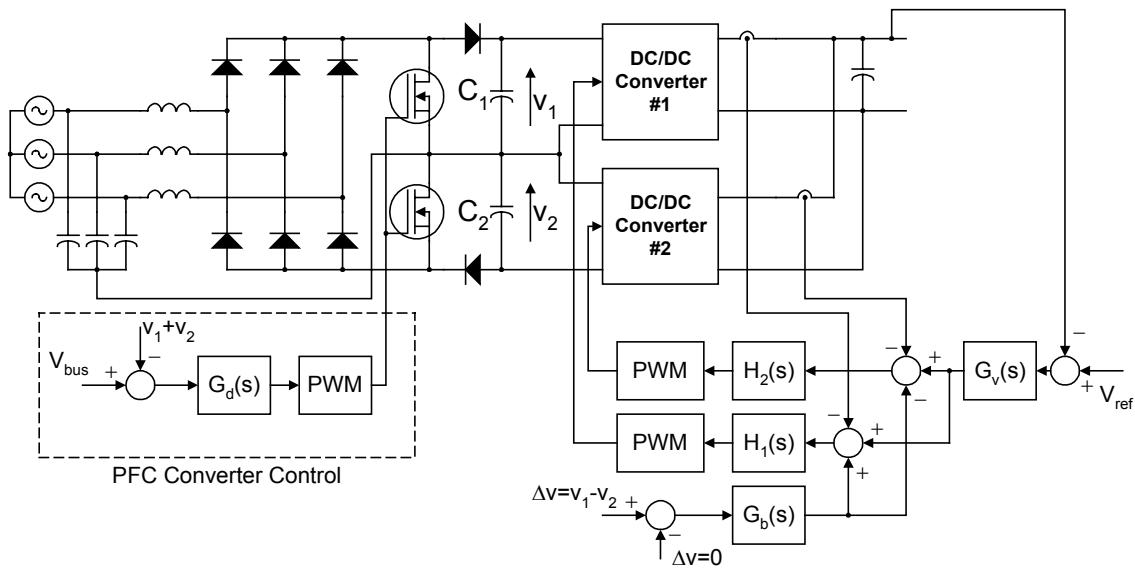
Fig. 3-5. Possible applications: (a) using two split DC/DC converters and (b) using a three-level DC/DC topology.

As shown in Fig. 3-5(a), if DC/DC converters are connected across the output capacitors of the three-level DCM boost rectifier, they can be used to balance the voltages across C_1 and C_2 . The

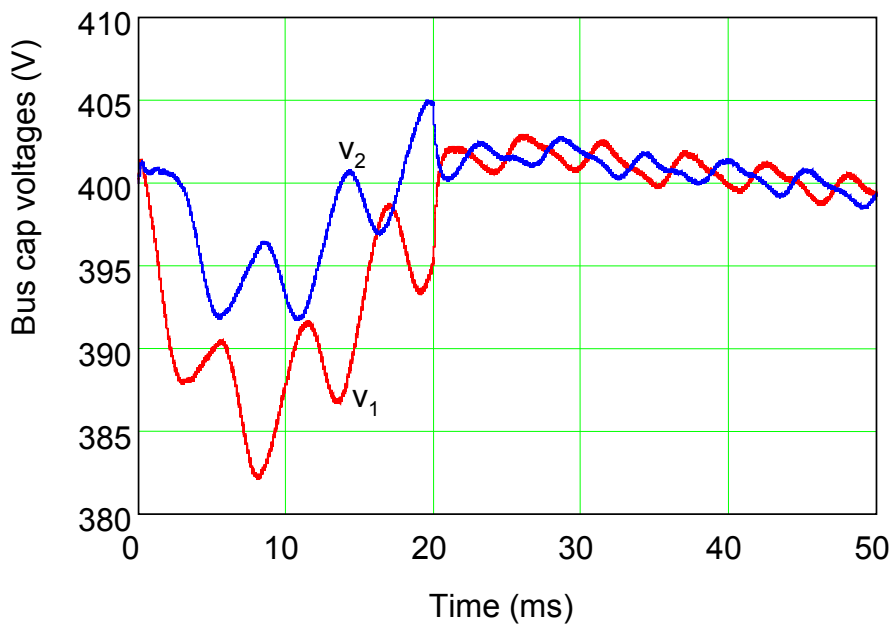
circuit diagram with a conceptual control scheme used to achieve voltage balance by controlling the DC/DC converters is illustrated in Fig. 3-6(a). As shown, a voltage controller is used to regulate the total bus voltage of the rectifier. The task of balancing the voltages v_1 and v_2 is then achieved by the two DC/DC converters. The control objective is to maintain the voltage difference $\Delta v = v_1 - v_2$ to as close to zero as possible. The output of the voltage balance regulator is added to or subtracted from the current reference of the DC/DC converters. As a result, both DC/DC converters will draw the right amount of power to maintain the voltage balance across the bus capacitors. This situation is shown in Fig. 3-6(b), where the bus capacitors have been set to $C_1 = 400\mu\text{F}$ and $C_2 = 500\mu\text{F}$. As shown in Fig. 3-6(b), after enabling the voltage balance compensator at $t = 20\text{ms}$, both voltages across C_1 and C_2 will be regulated to 400V despite the mismatch in the bus capacitance values. The simulation results show that the voltage balance method discussed in this paragraph is rather effective in balancing the voltages across the bus capacitors.

3.4. Converter Design Guidelines

Deriving design guidelines from the simplified circuit shown in Fig. 3-2 is relatively simple. However, in the practical circuit, the AC capacitors used to provide the artificial neutral point connection modify the voltage gain of the three-level boost rectifier, thus making it difficult to obtain a closed-form solution that enables one to obtain the design curves, as demonstrated in chapter 2 for the single-switch DCM boost rectifier. To simplify the problem of obtaining the voltage gain when the AC capacitors are connected to the circuit, a time-domain simulation can be used to determine the output characteristics of the rectifier.



(a)



(b)

Fig. 3-6. Using the DC/DC converters to control the voltage imbalance across the DC capacitors of the three-level DCM boost rectifier: (a) circuit diagram and (b) voltages across C_1 and C_2 .

The AC capacitors must be incorporated by the DM input filter. Therefore, typical values for the AC capacitances will range from $1\mu\text{F}$ to $3\mu\text{F}$. Fig. 3-7 shows the voltage gain as a function of the normalized output current obtained by simulation when the rectifier is operated at heavy load.

The simulation was performed such that the boost inductance and the duty cycle were iteratively adjusted to provide critical conduction at full load (6kW) and high-line input voltage (265V RMS line-to-neutral input voltage). Considering this approach, the rectifier operates as close as possible to the boundary line between CCM and DCM, which helps to reduce current stress in the devices. After adjusting the input inductance value, the input voltage was swept from high to low line (170V RMS line-to-neutral input voltage), while the output bus voltage was fixed at 800V. The duty cycle was then adjusted to provide full output power at a given input voltage. The results were then normalized and plotted in Fig. 3-7. Although the results shown in Fig. 3-7 were obtained for a specific power case, they can be directly used to design the two-switch three-level rectifier for any specification because the results have been normalized. The voltage gain and the normalized output current are defined as

$$(3-1) \quad M = \frac{V_o}{V_{pk}} \quad \text{and} \quad I_{norm} = \frac{I L f_s}{V_{pk}},$$

where V_o is the output bus voltage, V_{pk} is the peak line-to-neutral input voltage, I is the average output current, L is the boost inductance, and f_s is the switching frequency.

The design curve shown in Fig. 3-7 can be used to calculate the input inductance of the three-level DCM boost rectifier. As an example, suppose that the rectifier is designed to supply 3.15kW at 40kHz of switching frequency. The bus voltage is 800V, and the line-to-neutral input voltage is allowed to change from 170V to 265V RMS. From the specifications, the voltage gain of the PFC circuit at high-line input voltage is 2.14. From Fig. 3-7, the normalized output current results in 0.056, and from (3-1) the value of the boost inductance results in 133 μ H.

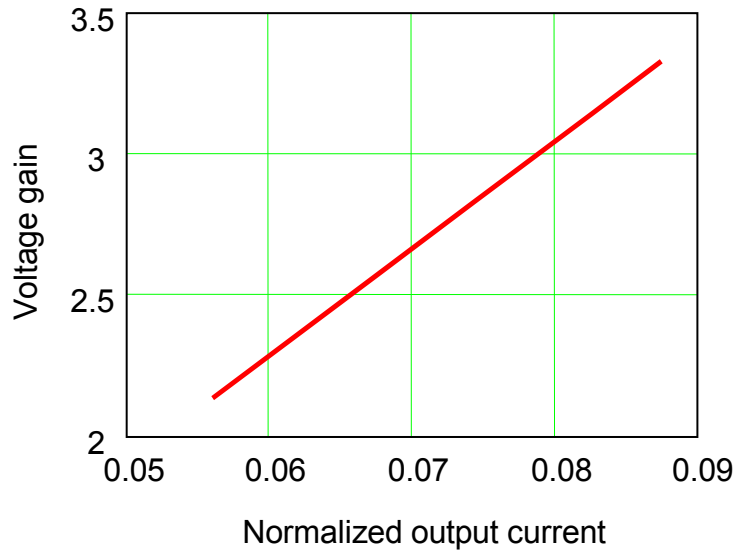


Fig. 3-7. Voltage gain versus normalized output current at heavy load.

3.5. Experimental Results and Comparisons

A prototype has been implemented and tested in order to validate the previously discussion. The two-switch three-level DCM boost rectifier shown in Fig. 3-1 has been implemented with the following devices: DSEI 30-10A (1000V/30A) for the three-phase input bridge diodes, DSEI 30-10A (1000V/30A) for the boost diodes, and APT60M75JVR (600V/62A) for the power MOSFETs. Although the total bus voltage is 800V, the three-level structure of the DCM boost rectifier enables the use of 600V devices or even 500V devices if the voltage margin is considered to be sufficient.

The current waveform in one of the boost inductors at 3kW of output power and 180V of input phase voltage is shown in Fig. 3-8(a). The DCM operation can be observed from the boost inductor current waveform. The three-level structure of the DCM boost rectifier is able to reduce

the voltage applied across the power switches to 50% of the total bus voltage, as shown for the switch S_1 in Fig. 3-8(b).

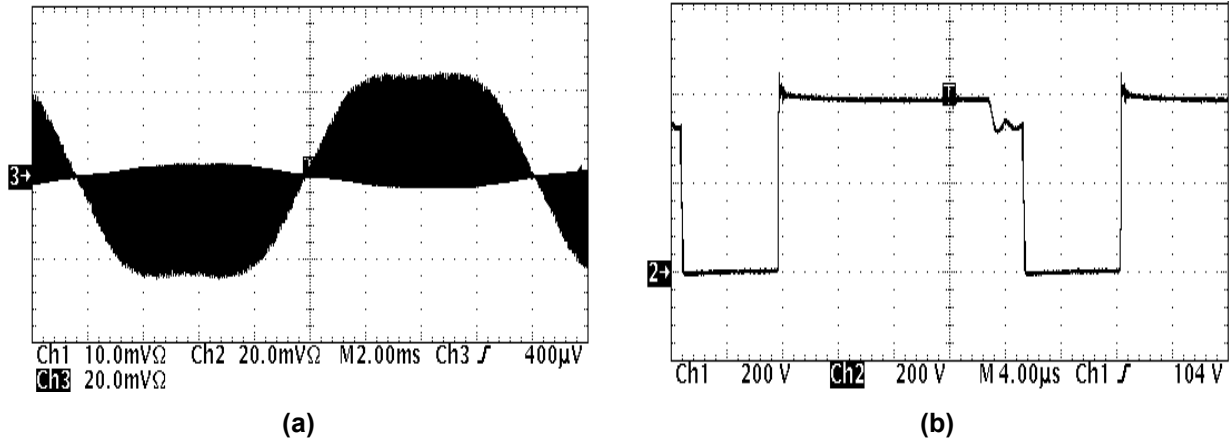


Fig. 3-8. Experimental results: (a) boost inductor current (10A/div) at 3kW and $V_{in}=180V$ and (b) voltage across one of the switches.

Fig. 3-9(a) shows the efficiency for two different designs: one at 40kHz and another at 70kHz. Since MOSFETs are used, the converter should be able to operate at higher frequencies as compared to the previous chapter in which IGBTs were switched at 40kHz. Including the input filter in the efficiency measurements, the efficiency is reasonably high for both switching frequencies. At nominal input phase voltage (220V line-to-neutral voltage), the efficiency of the two-switch three-level boost rectifier drops only 1% at 70kHz, as compared to the efficiency at 40kHz. The same figure also compares the efficiency of the two-switch three-level boost rectifier against the efficiency of the single-switch DCM boost topology discussed in the previous chapter. As can be seen, the two-switch three-level DCM boost rectifier outperforms its counterpart circuit.

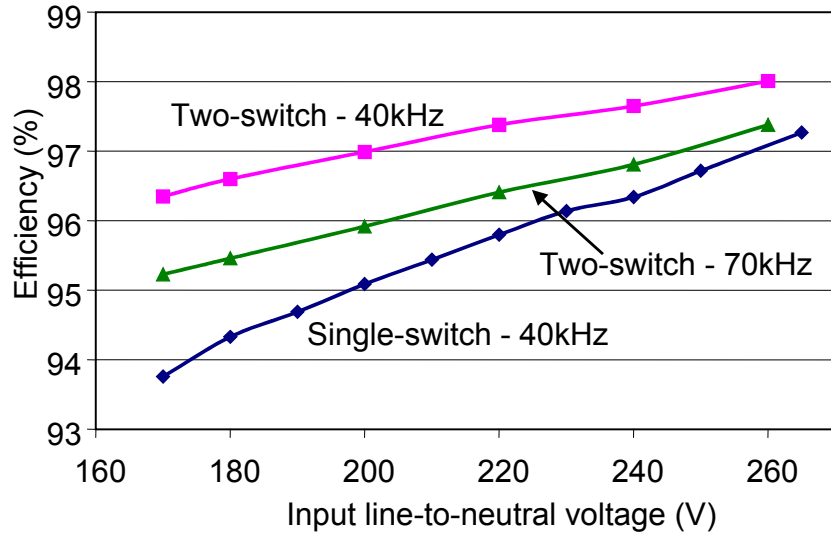
Fig. 3-9(b) shows the THD of the input currents as a function of the input phase voltage. The same figure also compares the THD of the two-switch three-level boost rectifier against the THD

produced by the single-switch three-phase boost topology. As can be observed, the two-switch three-level boost rectifier also presents lower THD. At nominal input phase voltage (220V), the THD of the two-switch three-level DCM boost rectifier is only 8.8%.

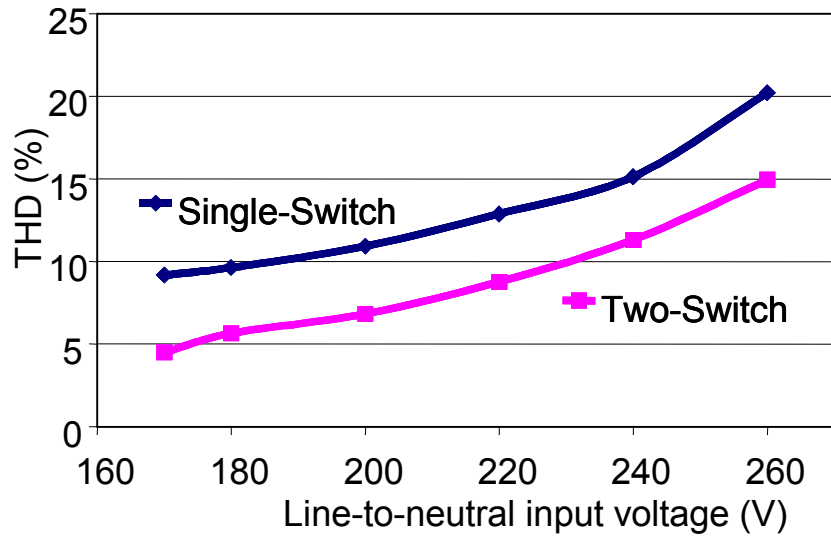
All the results illustrated in Fig. 3-8 and Fig. 3-9 show that the two-switch three-level DCM boost rectifier presents superior performance as compared to its counterpart discussed in the previous chapter.

3.6. Harmonic Injection Method

In order to decrease the THD to less than 10% over the entire input voltage variation (170V – 265V), the bus voltage of the two-switch three-level DCM boost rectifier must be increased to 890V. At this bus voltage, the 600V power switches can still be used with a considerable voltage margin. However, it is clear that increasing the bus voltage to reduce the THD of the input currents imposes serious restrictions on the bus capacitors, since they are usually chosen to support at most 450V. To overcome this problem, the harmonic injection technique can be applied to the two-switch three-level DCM boost rectifier to reduce the harmonic distortion of the input current [47]. A diagram of the system implementation using the harmonic injection method is shown in Fig. 3-10(a). According to what was presented previously [47], if the sinusoidal voltage across phase a is taken as the reference voltage for the three-phase system, then the modulated duty cycle applied to the two-switch boost rectifier can be written as



(a)



(b)

Fig. 3-9. (a) Efficiency comparison and (b) THD.

$$(3-2) \quad d_c = \frac{V_d}{V_{ramp}} \left[1 + m_h \sin \left(6\omega t + \frac{3\pi}{2} \right) \right],$$

where m_h is the modulation index of the harmonic injection signal, V_d is the output of the voltage compensator, and V_{ramp} is the peak voltage of the saw-tooth waveform generated by the PWM

controller. The THD generated by the two-switch three-level DCM boost rectifier using the harmonic injection method is given by

$$(3-3) \quad THD = \frac{\sqrt{(I_5 - m_h I_1)^2 - (m_h I_1)^2}}{I_1},$$

where I_1 is the fundamental input current and I_5 is fifth harmonic measured before the introduction of the harmonic injection. The minimum THD of the input currents can be achieved when

$$(3-4) \quad m_h = \frac{1}{2} \frac{I_5}{I_1}.$$

The main objective of using the harmonic injection method is to reduce the THD at high line. For the two-switch three-level DCM boost rectifier, the RMS fundamental current at 3.15kW and 265V is $I_1=4.15A$, while the fifth harmonic measured before the application of the harmonic injection method was 0.62A. From (3-4), m_h is set to 7.5% to minimize the THD at high line. Once m_h has been set to provide the minimum THD at high-line input voltage, the harmonic injection circuitry that is shown in Fig. 3-10(a) will then self-adjust the modulation index m_h for different operating points. The benefit of using the harmonic injection method in the two-switch three-level DCM boost rectifier can be seen in Fig. 3-10(b). As illustrated, the THD is reduced to 10% at high line, which represents a reduction of approximately five points with respect to the case without the harmonic injection implementation. At low-line input voltage, the THD of the two-switch three-level DCM boost rectifier using the harmonic injection method increases slightly, since the system becomes overcompensated by the self-adjusting modulation index.

Although there is a slight increase in the harmonic distortion at low-line when the harmonic injection method is applied, the THD remains below 10% at high line, while still maintaining the bus voltage at 800V.

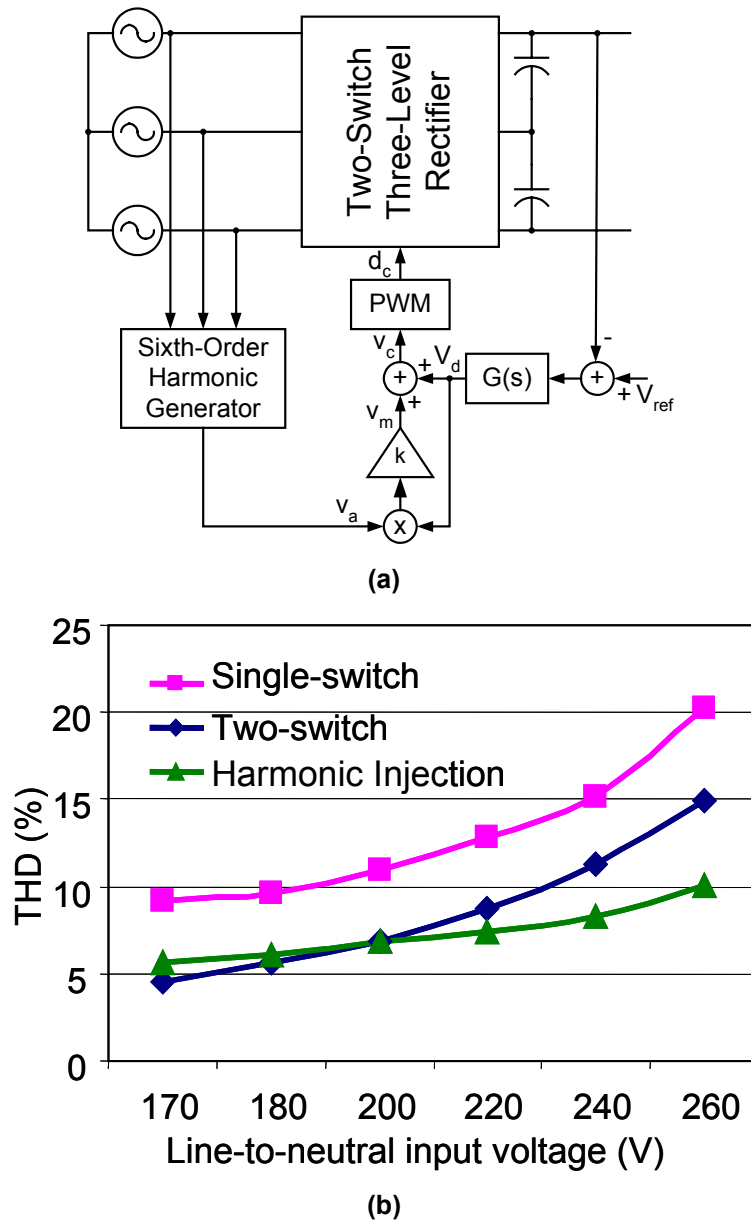


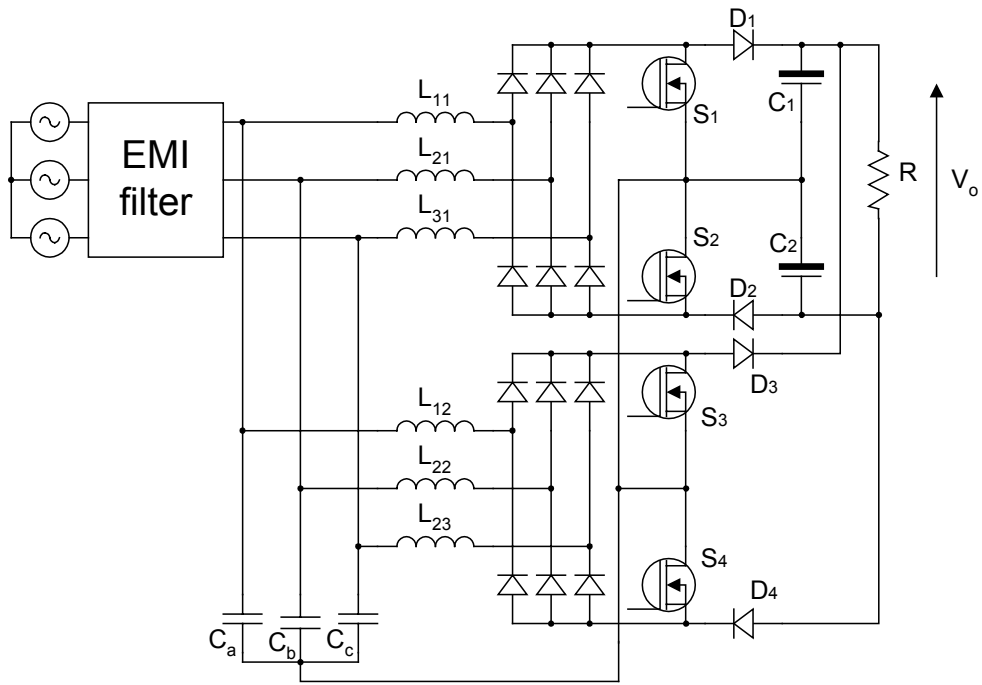
Fig. 3-10. The two-switch three-level DCM boost rectifier using the harmonic injection method: (a) implementation and (b) THD.

3.7. Input Current Ripple Cancellation

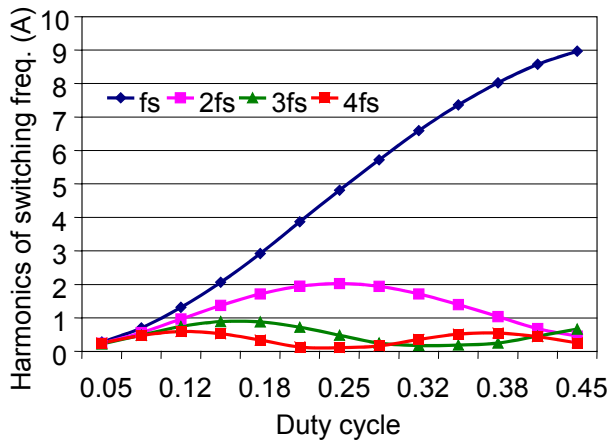
The converter discussed up to this point operates in DCM, and for this reason requires a large input filter to attenuate the input current ripple. Similar to what was discussed in the previous chapter, the interleaving technique can also be applied to reduce the amplitude of the input current ripple. An interleaved configuration using two rectifiers is shown in Fig. 3-11(a). Assuming that the interleaved system supplies 6.3kW of total power, according to section 3.4 each boost inductance shown in Fig. 3-11(a) should be 133 μ H at 40kHz.

Fig. 3-11(b) shows the amplitude of the main high frequency harmonics for a non-interleaved 6kW three-level DCM boost rectifier, while Fig. 3-11(c) shows the amplitude of the high-frequency harmonics when interleaving is applied to both three-level DCM rectifiers. The odd harmonics of the switching frequency are cancelled out by the interleaving effect. Therefore, the input filter can be designed to have a higher cutoff frequency in order to attenuate the current ripple. As can be observed, the effectiveness of the input current ripple cancellation is strongly dependent upon the operating duty cycle.

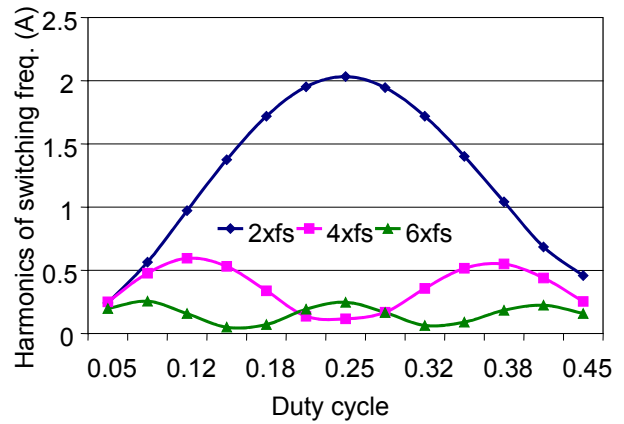
Fig. 3-12 shows the interleaved current waveform ($i_{L11}+i_{L12}$) at heavy load and for three different input phase voltages. The ripple cancellation provided by the two-channel interleaved three-level DCM boost rectifiers is quite effective. It can also be seen that there is a reduction in the ripple cancellation effectiveness as the input phase voltage increases, since the duty cycle decreases at high input voltage, which impairs the ripple cancellation effectiveness.



(a)



(b)



(c)

Fig. 3-11. (a) DCM interleaved two-switch boost rectifiers, (b) high-frequency harmonics without interleaving, and (c) high-frequency harmonics with interleaved operation.

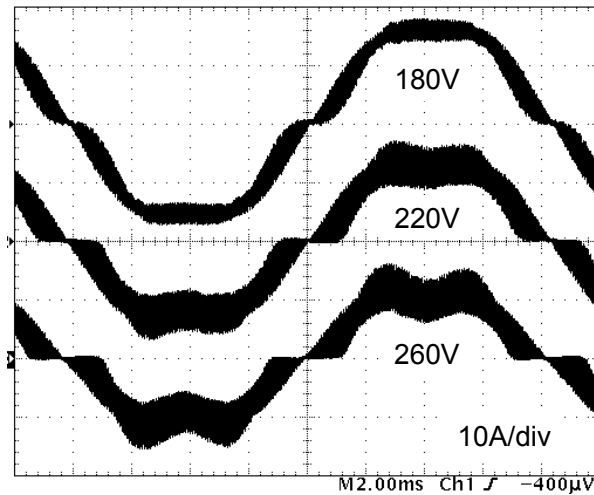


Fig. 3-12. Interleaved current at 6.3kW ($i_{L11}+i_{L12}$) (10A/div all traces) at three different input phase voltages.

3.8. DM Filter Parameters and Comparison

In this section, the parameters of the DM input filter are calculated and compared with those for the single-switch topology and both benchmark circuits (CCM boost and VIENNA rectifiers). Table 3-1 defines the operating point used for the DM filter design. The operating points for the non-interleaved and interleaved two-switch three-level DCM boost rectifiers are related to the worst-case input current ripple, and they have been extracted from the curves shown in Fig. 3-11(b) and (c).

3.8.1. DM Filter Parameters Evaluation for VDE 0871 Class B Standard

Fig. 3-13 shows the comparison of the DM filter parameters designed to attenuate the DM noise according to the VDE 0871 standard. The filter network used in the design is the same one introduced in the previous chapter (see page 56). The same assumptions are also taken into

account, such as neglecting the common-mode noise. A $6\text{dB}\mu\text{V}$ margin is also considered in the calculation of the filter parameters, while the total filter capacitance per phase is $3.8\mu\text{F}$.

Table 3-1. Identifying the DM filter design point (example: $f_s=40\text{kHz}$).

System	VDE 0871 Class B	CISPR 22 Class B
Two-Switch Non-Interleaved (6.3kW)	$V_{in}=170\text{V}$, $D=0.45$ and $P_o=6\text{kW}$ $f_{att}=40\text{kHz}$	$V_{in}=170\text{V}$, $D=0.117$ and $P_o=499\text{W}$ $f_{att}=160\text{kHz}$ ($4x f_s$)
Interleaved System (6.3kW)	$V_{in}=170\text{V}$, $D=0.25$ and $P_o=2.12\text{kW}$ $f_{att}=80\text{kHz}$ ($2x f_s$)	$V_{in}=170\text{V}$, $D=0.117$ and $P_o=499\text{W}$ $f_{att}=160\text{kHz}$ ($4x f_s$)
CCM Boost	$V_{in}=170\text{V}$ and $P_o=2\text{kW}$ $f_{att}=40\text{kHz}$	$V_{in}=170\text{V}$ and $P_o=2\text{kW}$ $f_{att}=160\text{kHz}$ ($4x f_s$)
VIENNA	$V_{in}=170\text{V}$ and $P_o=6\text{kW}$ $f_{att}=40\text{kHz}$	$V_{in}=170\text{V}$ and $P_o=6\text{kW}$ $f_{att}=160\text{kHz}$ ($4x f_s$)
Single-Switch Interleaved	$V_{in}=170\text{V}$, $D=0.25$ and $P_o=1.89\text{kW}$ $f_{att}=80\text{kHz}$ ($2x f_s$)	$V_{in}=170\text{V}$, $D=0.39$ and $P_o=4.4\text{kW}$ $f_{att}=160\text{kHz}$ ($4x f_s$)

Fig. 3-13(a) and Fig. 3-13(b) show the filter inductance requirements. Once again, it can be seen that interleaving makes a big difference in reducing the amount of filter inductance in order to provide the appropriate attenuation for the DM noise. Comparing the interleaved system based on the single-switch DCM boost rectifier with the one based on the two-switch three-level DCM boost rectifier, the results are quite similar. In fact, the interleaved system based on the three-level DCM boost rectifier requires slightly more filter inductance at low switching frequencies because the boost inductance of system studied in the previous chapter is $140\mu\text{H}$, while the boost inductance of the two-switch three-level DCM boost rectifier is $133\mu\text{H}$. This difference is reflected in a greater input current ripple for the two-switch three-level DCM boost rectifier, which explains the slight difference between the two interleaved systems.

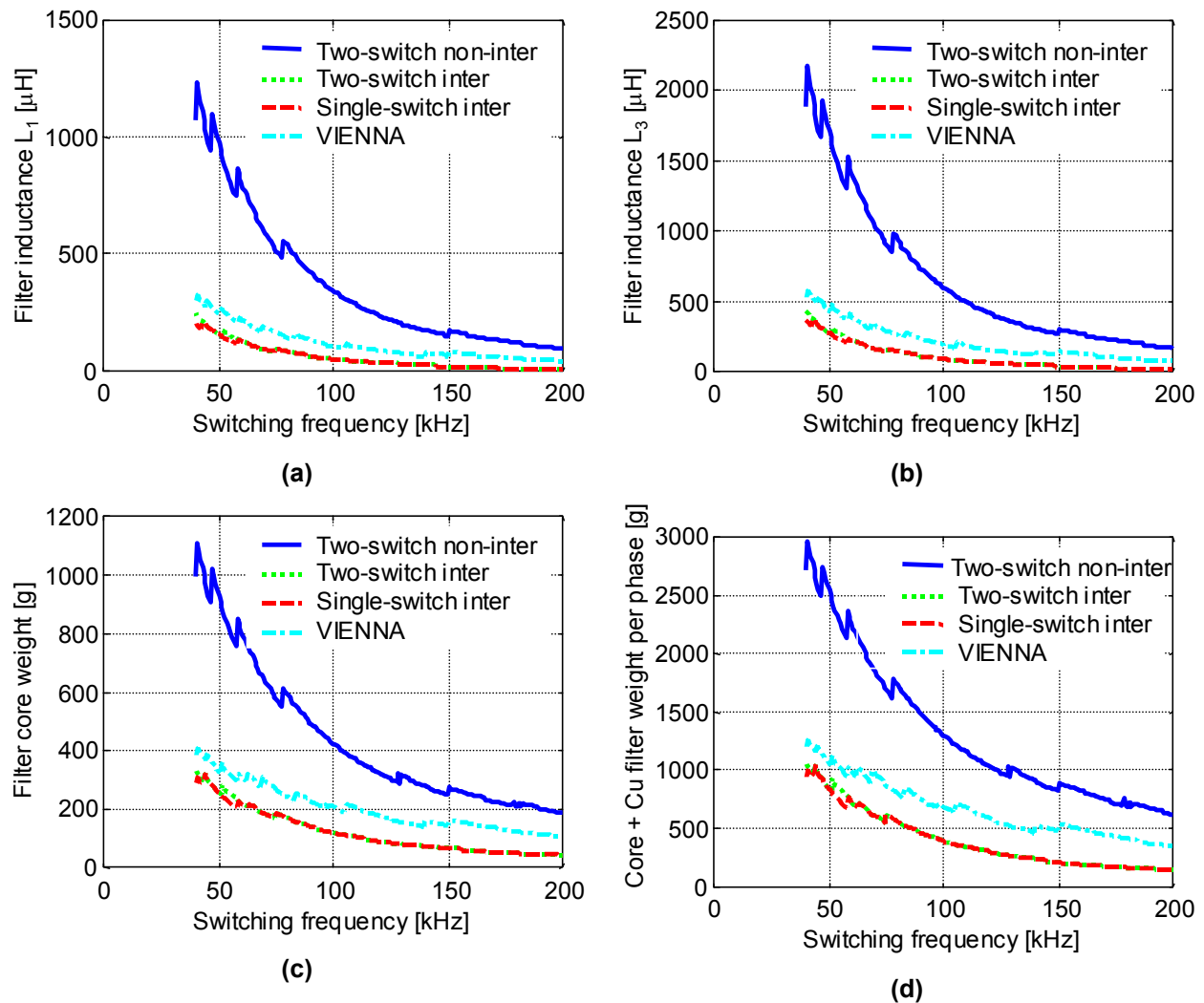


Fig. 3-13. Filter size for VDE 0871 Class B: (a) filter inductance L_1 , (b) filter inductance L_3 , (c) filter core weight to implement $L_d+L_1+L_3$, and (d) Core + Cu weight per phase required to implement $L_d+L_1+L_3$.

3.8.2. DM Filter Parameters Evaluation for CISPR 22 Class B Standard

The results of the evaluation are illustrated in Fig. 3-14. As can be seen, in terms of filter inductance and filter core weight, below a switching frequency of 150kHz, the VIENNA rectifier requires the smallest filter to attenuate the DM noise, while there is no clear benefit of interleaving the two DCM rectifiers. Between 50kHz and 150kHz of switching frequency, the

benefit of interleaving begins to show up over the non-interleaved case. The interleaving is beneficial for reducing the filter size above 150kHz. Although above 150kHz the interleaved systems require the least amount of filter inductors, the result is not as good as the VIENNA rectifier around 50kHz, 75kHz and 150kHz.

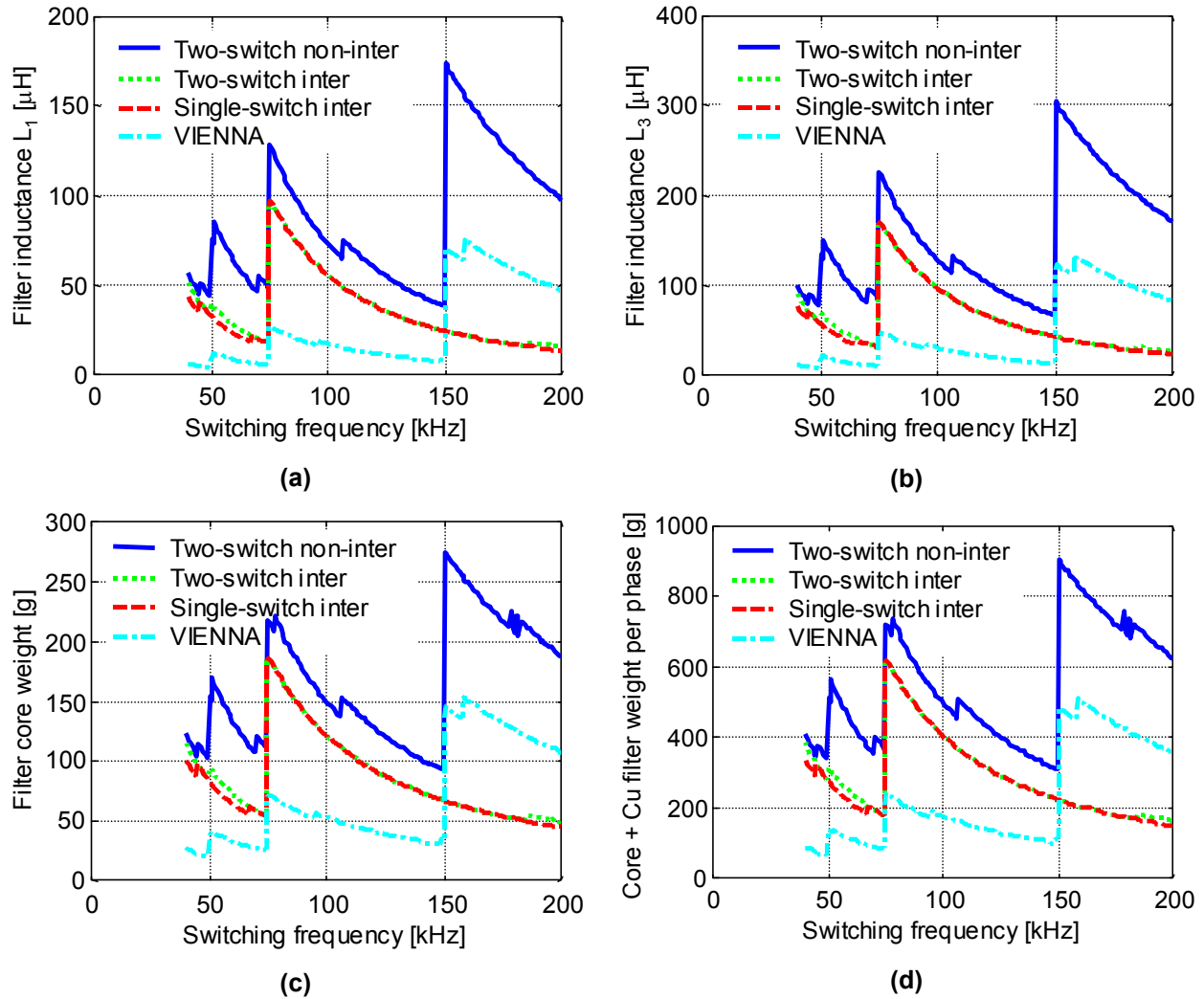


Fig. 3-14. Filter size for CISPR 22 Class B: (a) filter inductance L_1 , (b) filter inductance L_3 , (c) filter core weight to implement $L_d+L_1+L_3$, and (d) Core + Cu filter weight per phase required to implement $L_d+L_1+L_3$.

The benefit of interleaving the DCM boost rectifiers is obvious when the size of the boost inductor is combined with the size of the filter inductors, as shown in Fig. 3-15. The core weight for the boost and filter inductors is shown in Fig. 3-15(a). As can be seen, the interleaved rectifiers result in the lowest weight above 150kHz. However, for the switching frequency range between 50kHz and 75kHz, the interleaving technique also shows some benefit in reducing the combined boost and filter inductors sizes. In fact, designing the interleaving system so that it is slightly below 75kHz would be the best design point for minimizing the combined weight of the boost and filter inductors, since above 150kHz the switching frequency increases to such a point that soft-switching techniques must be implemented in the power switching stages. Fig. 3-15(b) includes the Cu weight needed to wind the boost and filter inductors. As can be observed, the conclusions remain the same when the Cu weight is included in the evaluation.

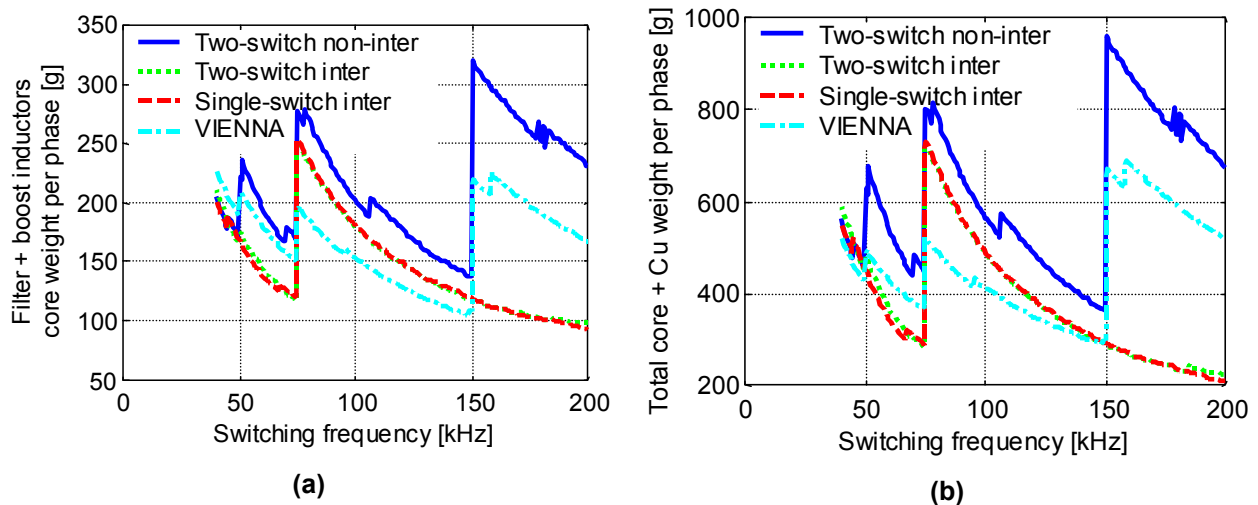


Fig. 3-15. (a) Combined filter and boost inductor core weight per phase and (b) total core + Cu weight needed to implement the boost and filter inductors per phase.

3.9. Common-Mode Noise Assessment

The results discussed up to this point have been based on the DM noise only. However, it is also important to understand the mechanisms under which the common-mode noise is generated and propagated through the various paths.

The identification of the disturbance sources and the propagation paths are essential steps towards understanding differential and common-mode noises in power electronics systems [66]. In this section, three different rectifiers are compared in terms of common-mode noise generation: (1) the single-phase CCM boost rectifier, (2) the VIENNA converter and (3) the two-switch interleaved DCM system. To compare the common-mode noise, a simulation was performed for the three circuits mentioned above by including parasitic elements in the component modeling. The next sub-sections describe the assumptions taken to model the various components of the topologies under consideration.

3.9.1. Modeling Boost Inductors

The boost inductors were modeled using PEmag, an Ansoft software component developed to model inductors and transformers [67]. The inductor model provided by PEmag is shown in Fig. 3-16. The equivalent model assumed for an inductor is the parallel connection of the inductance and the equivalent capacitance between turns. The boost inductor used in the CCM rectifiers (CCM boost and VIENNA) was designed at 40kHz using Micrometals T400/8 core size/material type [68], and having 103 turns wound with AWG 13 single strand Cu wire. Similarly, each boost inductor used in the two-switch three-level interleaved system was based on the T300/8

core size/material type, wound with 68 turns of AWG 16 single-strand Cu wire. The aspect ratio shown in Fig. 3-16 reflects the actual aspect ratio for each inductor. The Micrometals powder core was chosen to design the boost inductor because this material and the core sizes are already part of the PEmag library. Notice that both CCM rectifiers need one inductor per phase, while the interleaved system needs two inductors per phase to realize the circuit (two interleaved rectifiers). The PEmag simulation gives the parallel capacitance shown in Fig. 3-16.

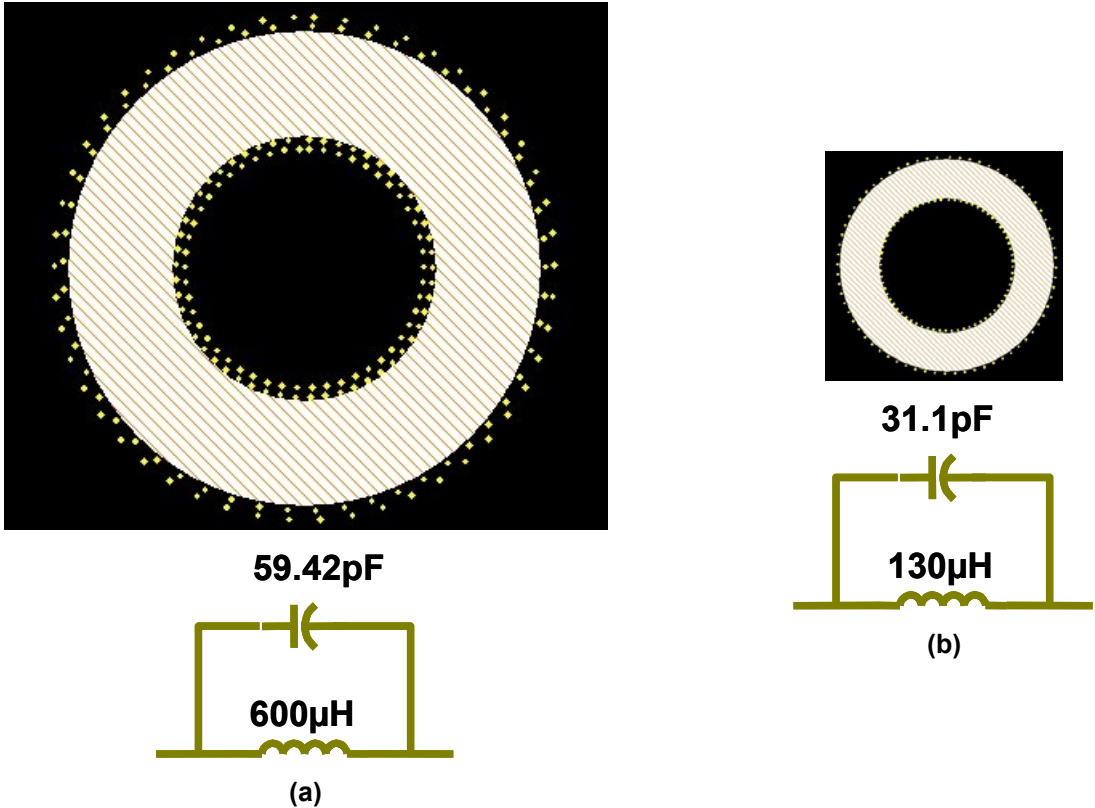


Fig. 3-16. Equivalent model for each boost inductor: (a) single-phase CCM boost and VIENNA rectifiers and (b) two-switch three-level interleaved system.

3.9.2. Parasitic Capacitance

The parasitic capacitance that connects the disturbance/noise source to the ground constitutes the major propagation path for the common-mode noise. The parasitic capacitance to ground depends heavily upon the circuit layout and how the power devices are mounted in the system. The assumption taken in this part of the analysis is that the power devices are mounted on the heat sink, which is connected to the ground, as illustrated in Fig. 3-17. To simplify the comparison, it is also assumed that all switches and diodes are packaged using the TO-247 standard package. Moreover, the devices are electrically isolated with a layer of mica. Having said that, the parasitic capacitance between the base plate of the device and the heat sink can be determined by using the following expression:

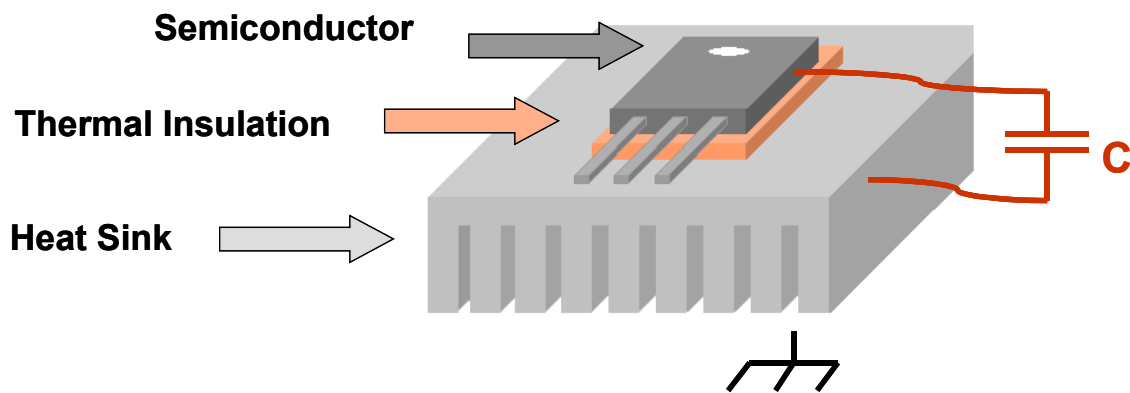


Fig. 3-17. Device assembly.

$$(3-5) \quad C_p = \frac{\epsilon_o \epsilon_r A}{d},$$

where ϵ_o is the permittivity of the air (8.85415×10^{-12} F x m), ϵ_r is the relative permittivity of the mica (4.5), A is the area of contact, and d is the thickness of the mica layer (0.25mm). From the

data above, the equivalent capacitance from the base plate of each device to the ground using the TO-247 package is 44pF.

3.9.3. Noise Propagation Paths

The disturbance sources for all cases under comparison are the voltages across the power switches. The dv/dt of these voltages are responsible for generating common-mode currents that flow through the parasitic capacitance. Fig. 3-18(a) shows the equivalent circuit of the single-phase CCM boost rectifier, including the parasitic capacitance of the boost inductor and the parasitic capacitance from the base plate of the MOSFET to the ground of the system. Every point oscillating at high frequency with respect to the ground is a potential propagation path for the common-mode noise current [66]. Taking this observation into account, the common-mode current will flow through the parasitic capacitance of the power MOSFET to the ground, as shown in Fig. 3-18(a). The VIENNA rectifier with the main parasitic components is illustrated in Fig. 3-18(b). As can be seen, the VIENNA rectifier presents many more possible paths for the common-mode noise, since all the points connected to parasitic capacitances oscillate at high frequencies during circuit operation. Finally, Fig. 3-18(c) shows the parasitic components considered for the two-switch three-level interleaved system.

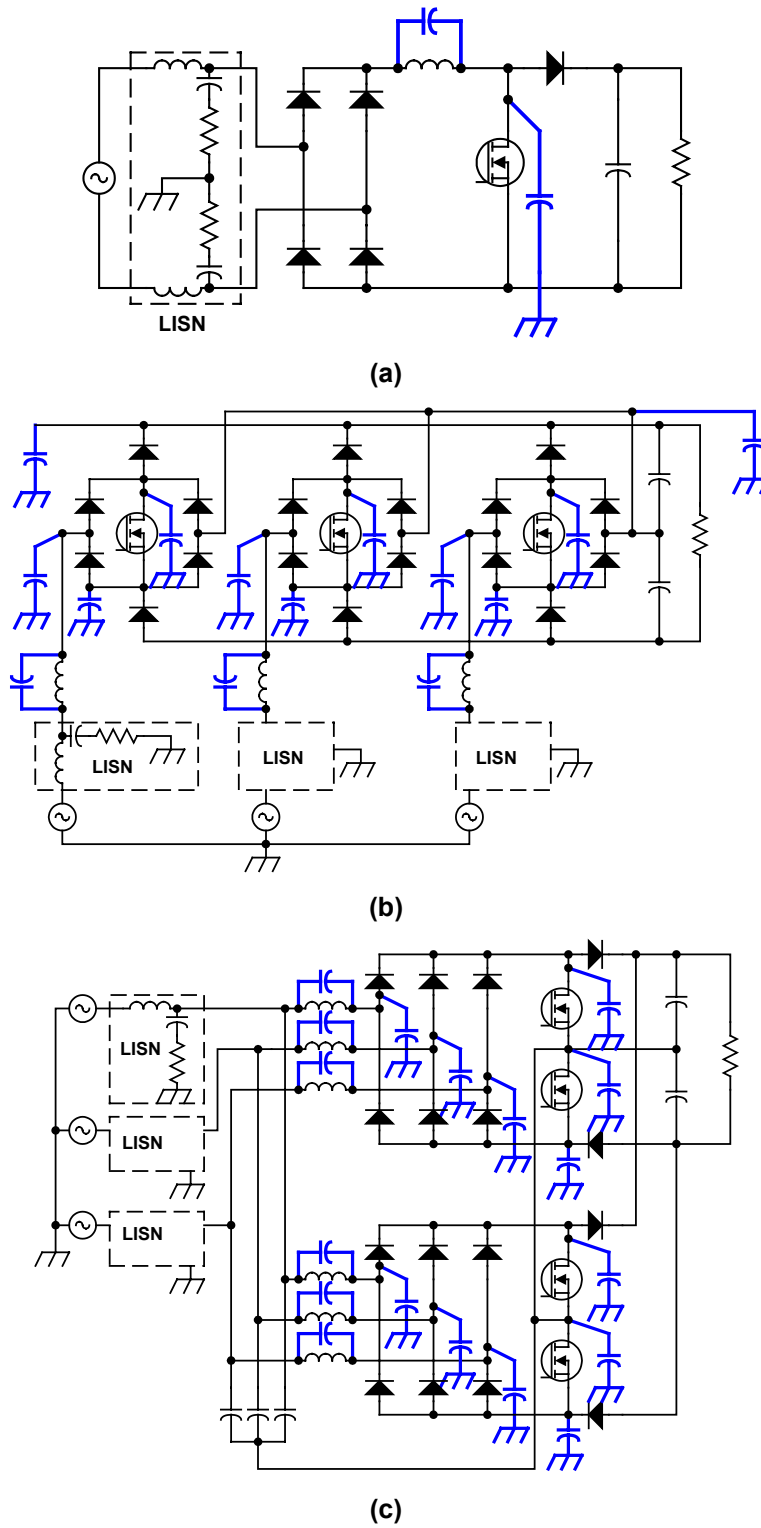


Fig. 3-18. Parasitic components: (a) single-phase CCM boost rectifier, (b) VIENNA rectifier and (c) two-switch three-level interleaved system.

The circuits shown in Fig. 3-18 were simulated in Saber under the following assumptions:

- The device models were taken from the Saber library.
- All circuits employed the same amount of Si per phase. For instance, the single-phase CCM boost rectifier used four switches in parallel. Since three single-phase modules are needed to build the system, the total number of switches is 12. To match the Si amount used in the CCM single-phase boost rectifier, the VIENNA rectifier was simulated with four switches in parallel per phase leg and the interleaved system with three switches in parallel to match a total of 12 switches. The MOSFET used in the simulation was the IRF540.
- It is assumed that the drain of the power MOSFET and the cathode of the diodes are connected to the base plate of the TO247 package. This assumption is important because it defines the connection point of the parasitic capacitance from each device to the ground.
- Based on the number of switches connected in parallel, the gate driver speed was adjusted to be the same for all cases. In this way, it is guaranteed that the dv/dt during fall and rise time is also the same.
- The neutral of the power system is grounded.

In order to compare the levels of common-mode (CM) noise generated by each case under comparison, the DM and CM noises should be separated from the total noise picked up by the 50Ω LISN impedance. Fig. 3-19(a) shows the equivalent setup used in the simulation of the single-phase CCM boost rectifier. From that equivalent setup, the DM and CM noises can be determined by

$$(3-6) \quad \begin{aligned} V_{DM} &= \frac{v_1 - v_2}{2} \\ V_{CM} &= -\frac{v_1 + v_2}{2} \end{aligned}$$

In a similar fashion, Fig. 3-19(b) shows the equivalent setup used in the simulations of the three-phase rectifiers. The separation of DM and CM noises in each phase can be obtained using the following relationships:

$$(3-7) \quad \begin{aligned} V_{a-DM} &= \frac{1}{3}(2v_1 - v_2 - v_3) \\ V_{b-DM} &= \frac{1}{3}(2v_2 - v_1 - v_3) \\ V_{c-DM} &= \frac{1}{3}(2v_3 - v_1 - v_2) \\ V_{CM} &= -(v_1 - v_2 - v_3) \end{aligned}$$

Although the phase angle for each DM noise harmonic is different because of the three-phase system, the amplitude of the DM noise in each input phase is the same.

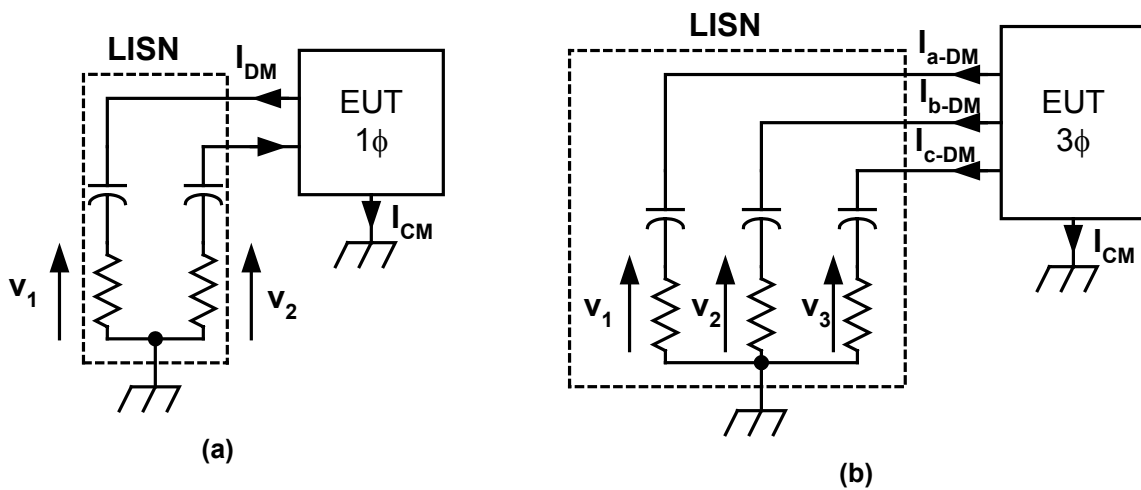


Fig. 3-19. Equivalent high-frequency noise path: (a) single-phase and (b) three-phase.

The Saber simulation results are plotted in Fig. 3-20, showing that the CCM boost rectifier generates the lowest level of CM noise, while the interleaved system generates the largest level at $2xf_s$. Notice that the interleaved system has a concentrated harmonic at $2xf_s$, while the CCM boost and VIENNA rectifiers show a more scattered spectrum of harmonics because of the severe reverse recovery of the fast diodes, as opposed to the interleaved system that presents no reverse recovery, explaining why the spectrum is more concentrated at $2xf_s$. The CCM boost rectifier presents nearly the same noise amplitude between 80kHz to 400kHz, while for the VIENNA rectifier this frequency range occurs between 80kHz and 300kHz. Although the previous DM input filter comparison results showed that it is more advantageous to design the interleaved system between 50kHz and 75kHz, the same results also presented limited meaning because the CM filter has not been taken into account in the comparison. However, it is clear from the simulation results shown in Fig. 3-20 that the interleaved system also requires lower CM filtering than the CCM boost and VIENNA rectifiers.

3.10. Device Stress Comparison

Fig. 3-21 illustrates three categories of device stress: average switch current, RMS switch current, and RMS bus capacitor current. As can be seen, the switches of the interleaved systems present similar average and RMS currents, as compared to the CCM boost and VIENNA rectifiers. Regarding the voltage stress, the single-switch DCM boost rectifier must support the highest voltage stress (800V). The CCM boost PFC and the VIENNA rectifier can be realized with 500V MOSFETs, while the interleaved system based on the two-switch three-level DCM boost rectifier can be realized with 600V devices.

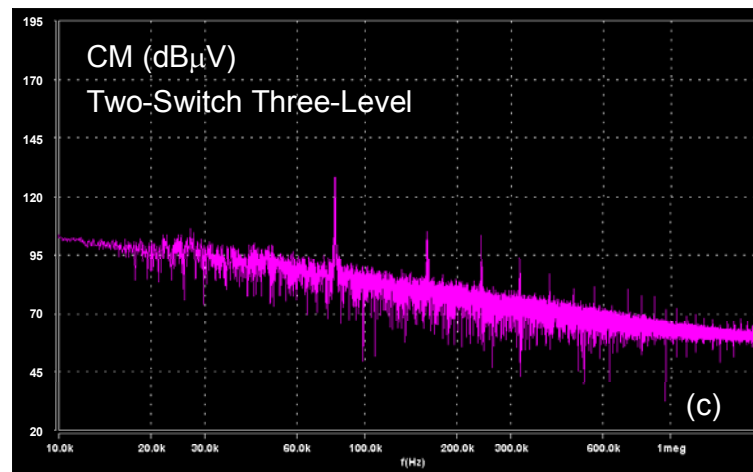
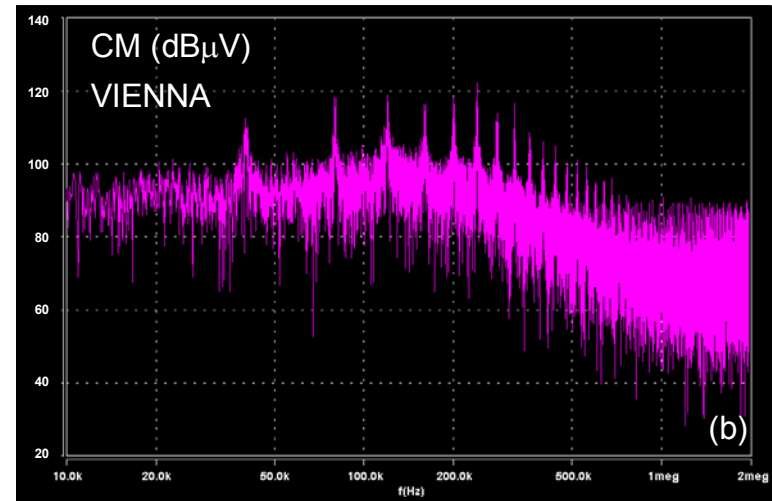
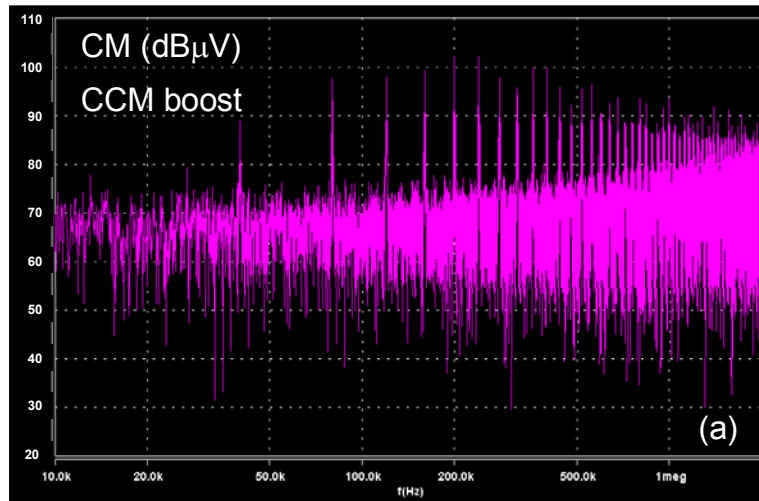


Fig. 3-20. CM noise generated by the various converters: (a) CCM boost, (b) VIENNA and (c) interleaved.

Fig. 3-21(c) shows the RMS current of the bus capacitors for the converters under comparison.

As can be verified, both interleaved systems present the lowest RMS bus capacitor currents of all the converters under comparison

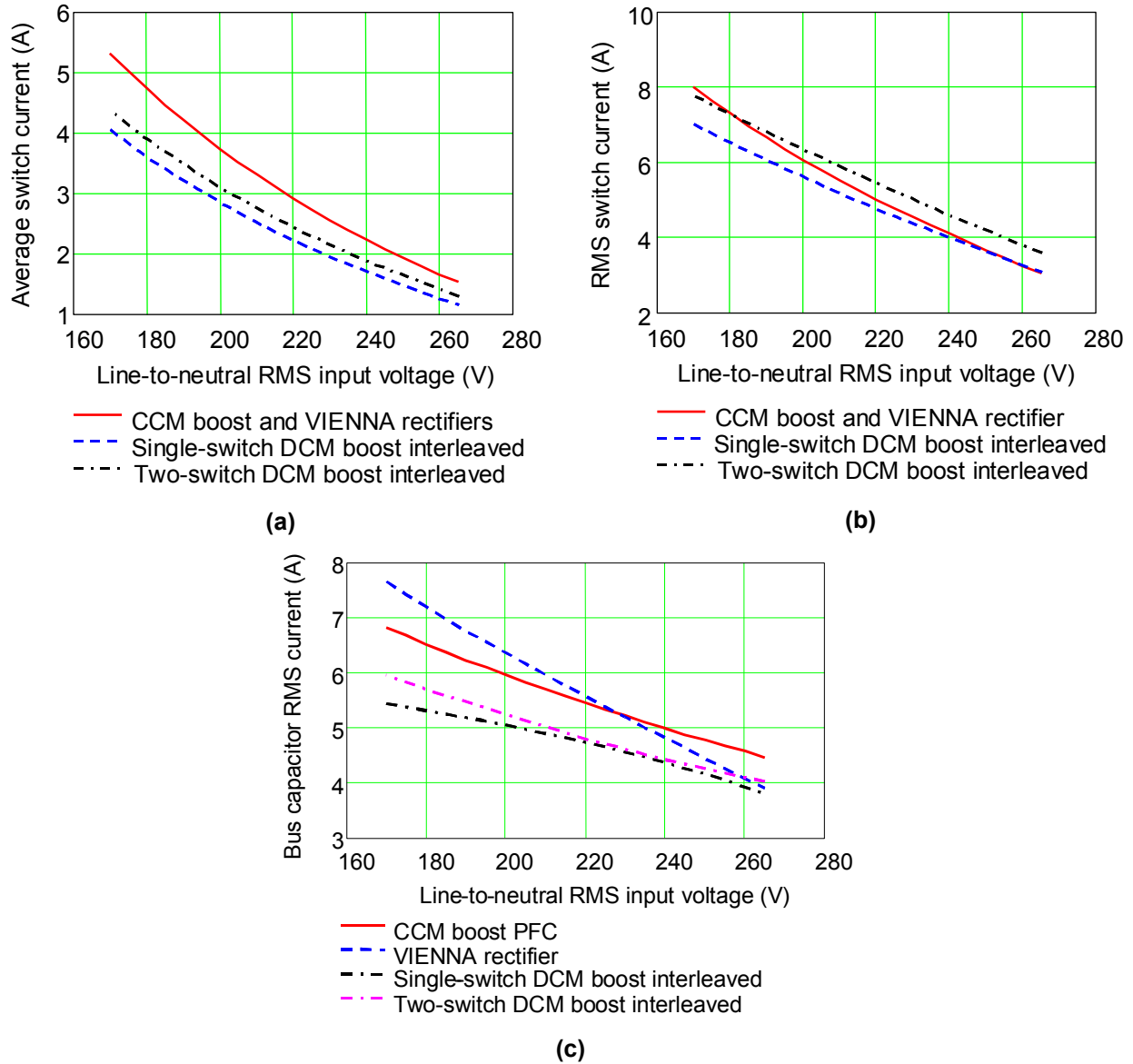


Fig. 3-21. Device stress: (a) average switch current, (b) RMS switch current and (c) RMS bus capacitor current.

3.11. Efficiency Comparison via Simulation Tool

Since the 2kW single-phase CCM boost PFC and the 6kW VIENNA rectifier were not prototyped for operational tests, a viable method for comparing the efficiency was to perform a simulation of the converters based on the loss models developed for MOSFETs and diodes using Simplis [69] [70].

The assumptions made are similar to those in the previous section. For instance, the same amount of Si was used per phase in all the converters, which resulted in a total of 12 switches evenly distributed among the phases of each approach. The gate driver was then adjusted to reproduce the same switching speed in order to make a meaningful comparison of switching losses. As seen in Fig. 3-22, the interleaved system performs very well as compared to the CCM and VIENNA rectifiers. The core and winding losses of the boost inductors were not included in the evaluation results illustrated in Fig. 3-22, while the switching frequency used in the evaluation was 40kHz and the total power was 6kW.

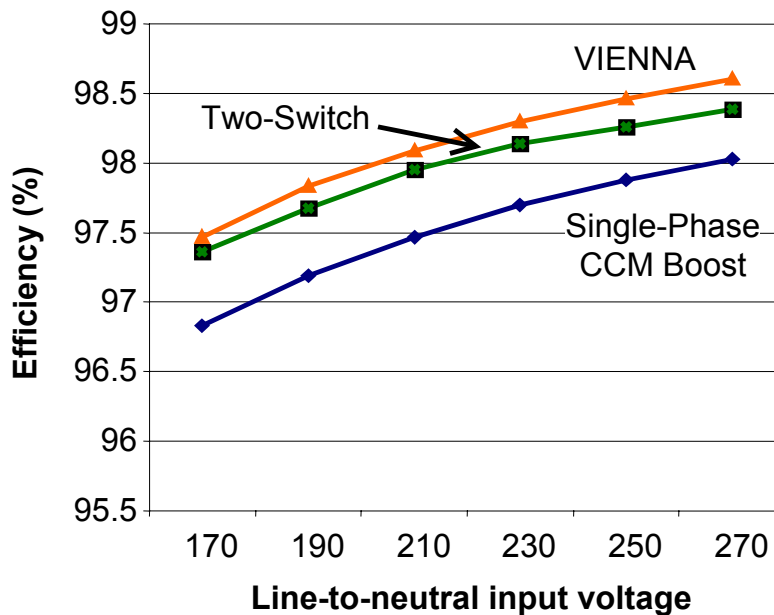


Fig. 3-22. Efficiency comparison.

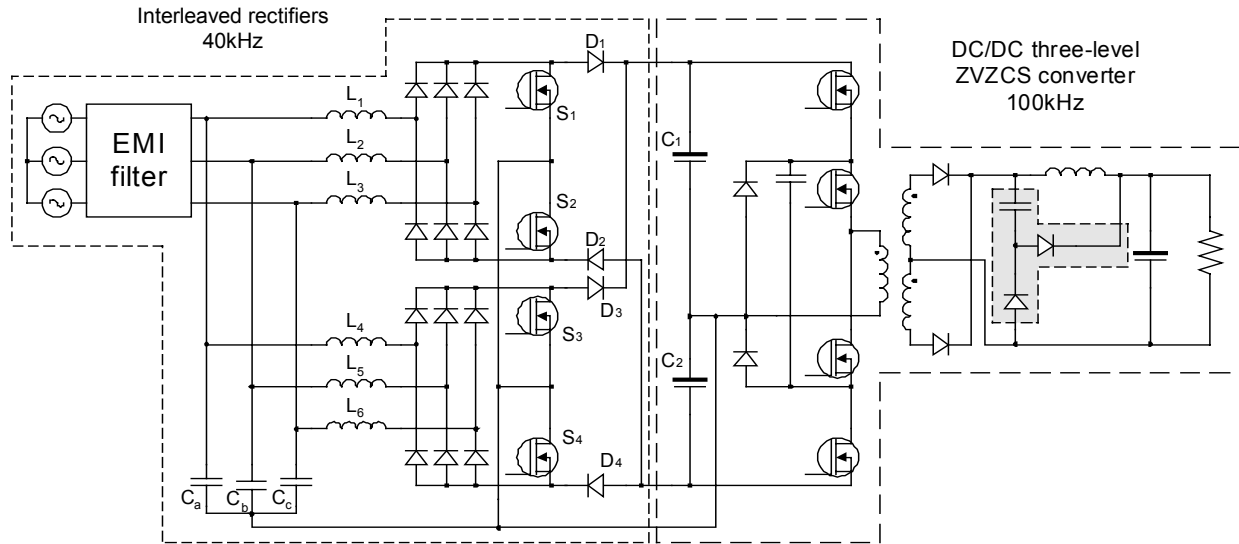
3.12. Two-Stage Front-End Converter Based on the Interleaved Two-Switch Three-Level DCM Boost Rectifier

The ultimate objective is to build a two-stage system that can supply 6kW of power at 48V of DC output voltage for telecom applications using the two-switch interleaved system in the PFC stage. Fig. 3-23(a) shows the front-end converter implemented with the two-switch three-level interleaved DCM boost rectifiers, followed by a three-level DC/DC converter implemented with the ZVZCS technique briefly discussed in the previous chapter. Fig. 3-23(b) shows the experimental efficiency comparison between the system developed in this chapter and the one developed in the previous chapter using the interleaved single-switch DCM boost rectifier. Even when operating the two-switch three-level interleaved system at 70kHz, the overall efficiency of the system (including the DM input filter) is still higher than the efficiency of the two-stage converter discussed in the previous chapter. Moreover, a switching frequency of 70kHz has been demonstrated as one of the best switching frequencies for reducing the size of the combined boost and filter inductors, as illustrated in Fig. 3-15 (b).

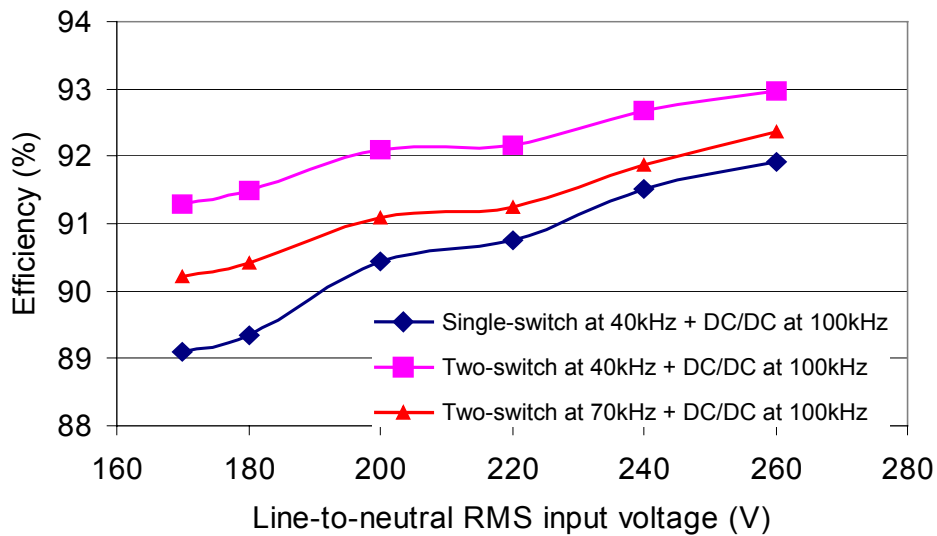
3.13. Benchmarking

Table 3-2 shows a comparison summary between the benchmark circuits and both DCM boost rectifiers studied to this point. As can be seen, the two-switch three-level DCM boost rectifier presents substantial improvements over the single-switch DCM boost rectifier in terms of switch voltage, efficiency, and THD. The DCM boost rectifiers also present reduced RMS bus capacitor current, while the power transferred under two-phase operation is almost the same as the benchmark circuits. The other points in favor of the DCM boost rectifiers are the sensing effort

and the control complexity. The two-switch three-level DCM boost rectifier improved the THD, but it is not yet possible to achieve the performance of the benchmark circuits.



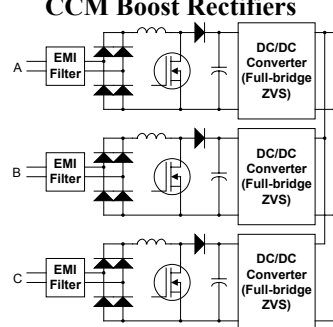
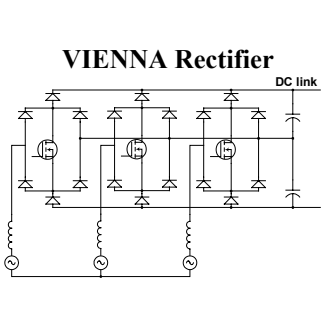
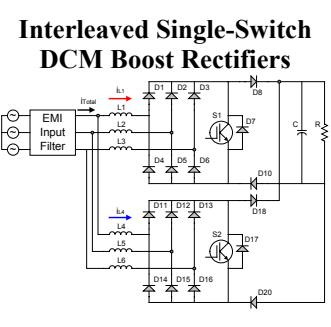
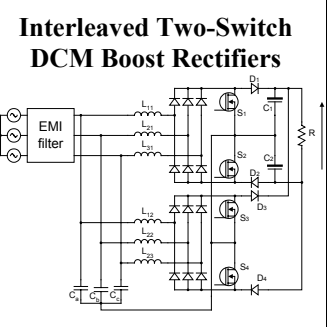
(a)



(b)

Fig. 3-23. (a) Two-stage front-end converter and (b) experimental efficiency comparison.

Table 3-2. Benchmarking the two-switch three-level DCM boost rectifier ($V_{in}=220V$ LN) .

<div style="text-align: center;">Topology</div> <div style="text-align: center;">Feature</div>	<div style="text-align: center;">CCM Boost Rectifiers</div> 	<div style="text-align: center;">VIENNA Rectifier</div> 	<div style="text-align: center;">Interleaved Single-Switch DCM Boost Rectifiers</div> 	<div style="text-align: center;">Interleaved Two-Switch DCM Boost Rectifiers</div> 
Total power (kW)	6	6	6	6
Switches	3	3	2	4
Line freq. diodes	12	12	-	-
Fast diodes	3	6	16	16
Bus voltage (V)	400	800	800	800
Switch voltage (V)	400	400	800	400
RMS/AVG SW current (A)	5.5/3.2	5.5/3.2	4.9/2.3	5.5/2.5
AVG diode current				
Line freq. Diodes (A)	4.1	4.1	-	-
Fast diodes (A)	5	2.5	4.1 (input rec.) – 3.75 (output)	4.1 (inp. rec.) – 3.75 (output)
Output cap RMS current (A)	5.5	5.6	4.75	4.75
Bus cap(μF)/Energy(J)	3x660/158	2x230/37	36/12	2x136/22
THD (%)	-	-	12.7	8.8
THD with harmonic injection (%)	-	-	10.8	7.4
Efficiency (%) at 40kHz	98 (simulation)	98.2 (simulation)	95.8	97.4
Power under two-phase operation (kW)	4	4	3.4	3.6
Active current control	Yes	Yes	No	No
Sensing effort	Medium	High	Low	Low
Control complexity	High	High	Low	Low

3.14. Conclusion

This chapter presented the two-switch three-level DCM boost rectifier as an alternative for PFC in DPS applications. The advantage of three-level topologies is the 50% reduction of the voltage applied across the power switches. As a result, lower-voltage devices such as MOSFETs with low on-resistance can be used to improve the rectifier performance. MOSFETs can also operate at higher switching frequencies in order to reduce the size of magnetic components, such as the boost and filter inductors.

As demonstrated, the two-switch three-level DCM boost rectifier achieves an efficiency of 97.4% at 40kHz and 96.4% at 70kHz. Both efficiencies, measured at 220V of input phase voltage, outperform the efficiency of its counterpart single-switch DCM boost rectifier, which achieved 95.8% at 40kHz. The THD of the two-switch three-level DCM boost rectifier is almost five points lower than the THD of the single-switch DCM boost rectifier. It was shown that the implementation of the harmonic injection method helped to reduce the THD to below 10% over the entire input voltage variation.

The interleaving technique also demonstrated benefits in reducing the DM filter size of the two-switch three-level DCM boost rectifier. The DM filter size reduction achieved by interleaving two rectifiers was clear when the filter was designed to attenuate the DM noise according to the VDE 0871 Class B standard. However, when the CISPR 22 was used, the benefit of filter size reduction was not as obvious, except when the switching frequency was increased above 150kHz. Below this switching frequency, the VIENNA rectifier was clearly more advantageous. The combined size of the boost and filter inductors then showed that interleaving the DCM boost rectifiers is indeed effective in reducing the requirements for magnetic components. In fact,

increasing the switching frequency to approximately 75kHz was demonstrated to be the optimal point at which to design the interleaved system in order to minimize the size requirements for the boost and filter inductors. Between 75kHz and 150kHz, there are no advantages in using interleaving to reduce magnetic component size. Above 150kHz, the interleaving of two DCM boost rectifiers again becomes attractive, but then the higher switching losses that occur due to higher switching frequencies become a challenge.

4. Single-Stage Three-Phase AC/DC Front-End Converters

4.1. Introduction

The discussions of the previous chapters revolved around the two-stage approach for front-end converters, which started with single-phase modules to configure a high-power system, and then progressed towards three-phase approaches, such as the VIENNA rectifier, for applications above 6kW. Possible solutions for reducing the cost of the front-end PFC were presented, such as the single- and two-switch DCM boost rectifiers. Such PFC configurations were also interleaved to help reduce the combined size of boost and filter inductors.

As an alternative solution, the PFC and DC/DC converters can be integrated into one power stage to reduce the front-end converter cost, as described in previous work [71]-[74]. These solutions, except for one [71], cannot handle very high power levels because they use single-switch topologies, such as the three-phase cuk, zeta and flyback converters. Moreover, these topologies are well known for increasing the voltage stress across the switch. In one solution [71], a phase-shift full-bridge topology was used to implement a single-stage converter. Despite the need for an auxiliary transformer winding that operates as a magnetic switch to control the PFC function, the overall system [71] is simpler than those discussed in the previous chapters. However, the single-stage converter previously presented requires the power switches to withstand the total intermediate bus voltage stress [71]. This problem turns out to be critical, since the intermediate bus voltage in single-stage converters fluctuates according to input voltage and load variations. Therefore, power switches with high voltage ratings are required if the

converter is intended to operate in power systems in which the nominal line-to-neutral voltage is 220V.

To overcome this problem, the work presented in this chapter proposes novel three-phase and three-level single-stage AC/DC converters that are able to achieve low harmonic distortion and reduced parts count, as well as to reduce cost when compared to those solutions discussed in the previous chapters. The proposed three-level converters discussed in this chapter decrease the voltage stress across the power switches, achieve ZVS without auxiliary circuits, and require only four switches to perform the featured functions.

This chapter presents a comparison of different approaches for single-stage three-phase AC/DC power conversion. Different aspects are compared throughout the chapter, such as intermediate bus voltage stress, harmonic distortion, efficiency, interleaved operation, and ability to constrain psophometric noise.

4.2. Single-Stage Approach

In a two-stage approach, the rectifier and DC/DC converter operate independently from each other because the intermediate bus capacitor is large enough to decouple the operation and the control of both stages, as illustrated in Fig. 4-1. The advantage of the two-stage approach is that the PFC circuit provides a regulated intermediate bus voltage (800V in this case), which facilitates the design optimization of both converters with respect to efficiency. Since in a two-stage front-end converter the design of both stages can be more easily optimized, the overall performance is improved as compared to a single-stage topology. Therefore, the main reason to

pursue single-stage solutions for AC/DC power conversion applications is the potential for cost reduction.

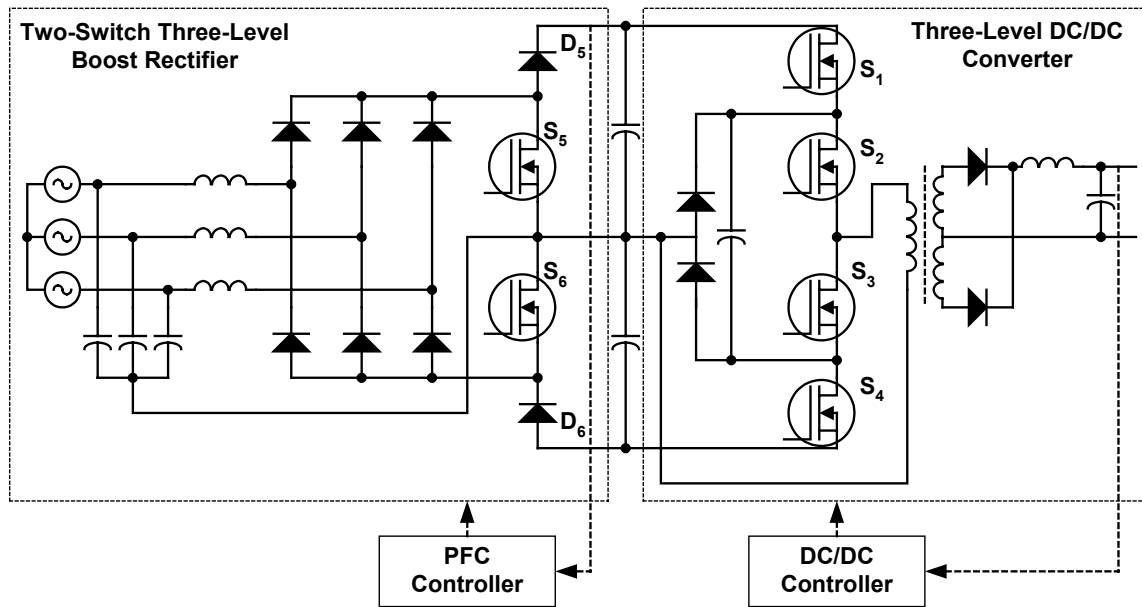


Fig. 4-1. Two-stage front-end converter using three-level topologies.

The single-stage approach can reduce cost because of the reduced number of switches and controllers needed to shape the input current and to regulate the DC output voltage [75] [76]. Although the cost of single-stage front-end converters is lower than that of a two-stage approach, the intermediate bus voltage can no longer be regulated because the controller in the circuit is used to regulate only the DC output voltage. Consequently, the variation of the intermediate bus voltage creates detrimental effects in terms of the overall efficiency optimization.

It is envisioned that with increased power levels for mainframe computers and servers, lower-cost solutions will become more in-demand in the future. Trying to address the ever-increasing requirement for lower-cost applications, this chapter addresses the functional integration of PFC and DC/DC converters into a single stage of power conversion.

4.3. Synthesis of the Single-Stage Three-Level Phase-Shift (TL-PS) Front-End Converter

The main objective for integrating the power stages is to eliminate both switches S_5 and S_6 and diodes D_5 and D_6 from the PFC stage shown in Fig. 4-1. There are very few steps necessary for the integration of the power stages. The first step is to eliminate the devices S_5 , S_6 , D_5 and D_6 from the PFC stage shown in Fig. 4-1. The second step is to connect the output of the three-phase input bridge to the positive and negative DC rails, as illustrated in Fig. 4-2(a). As can be seen in the same figure, the PFC function can no longer be performed because of the way the artificial neutral is connected to the power stage. In fact, the input section would operate as a conventional bridge-type rectifier supplying a capacitive filter, which would require huge input peak currents to charge the bus capacitors. To overcome this problem, the third step in the synthesis of the single-stage converter is to move the artificial neutral point connection to point B. The result of reconnecting the artificial neutral point is shown in Fig. 4-2(b). The four switches that remain in the circuit operate with phase-shift control to transfer power to the output, as well as to store energy in the input inductors designed to operate in DCM. Fig. 4-3 shows the main operating waveforms of the proposed converter.

4.3.1. Circuit Description and Operating Stages

This section presents the operating principle of the proposed single-stage TL-PS converter. The converter shown in Fig. 4-2(b) contains four power switches S_1 to S_4 , three input boost inductors L_a to L_c , two intermediate bus capacitors C_{b1} and C_{b2} , two clamping diodes D_{c1} and D_{c2} , a clamping capacitor C_f for ZVS operation of the outer switches, two output rectifiers D_{r1} and D_{r2} , an output filter consisting of L_o and C_o , and a transformer that isolates the output voltage from

the three-phase input. A resonant inductor L_r has been placed in series with the primary side of the transformer to increase the load range with soft-switching operation. The capacitors C_a , C_b and C_c provide an instantaneous three-phase voltage source and an artificial neutral point connection to avoid circulation of zero-sequence-order harmonics in the power lines. The AC capacitors used to provide the artificial neutral point connection are not extra components, since they are incorporated by the EMI filter.

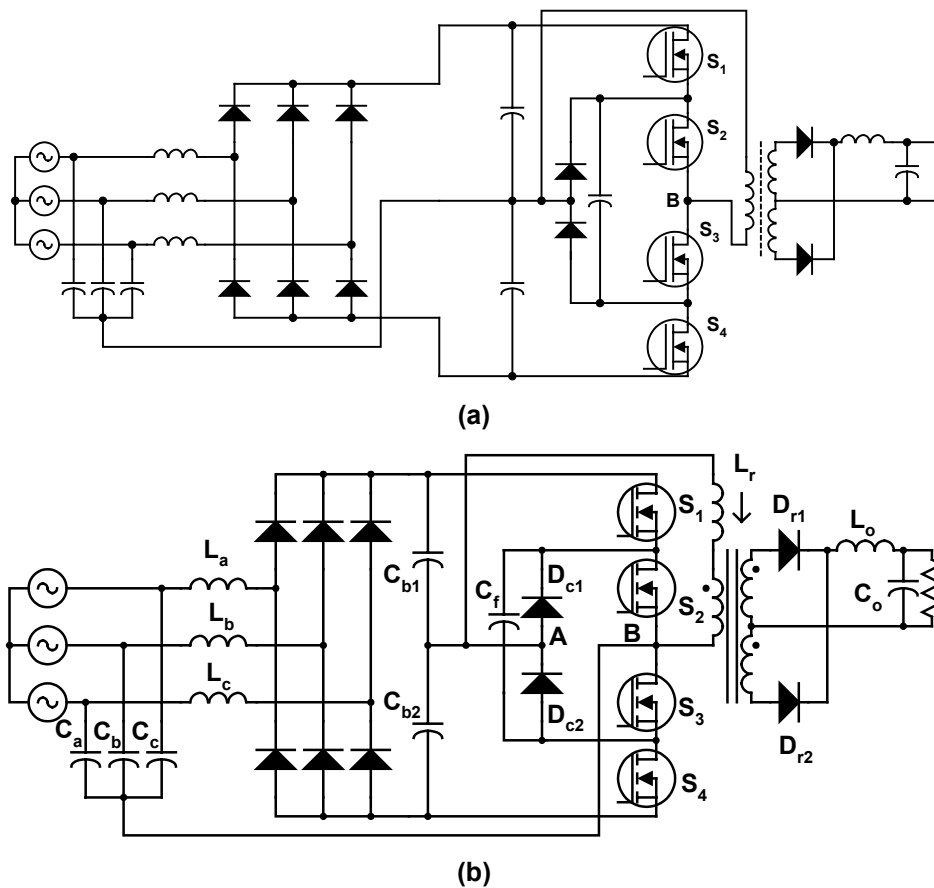


Fig. 4-2. Synthesis of TL-PS single-stage AC/DC converter: (a) eliminating the PFC cell, and (b) reconnecting the artificial neutral point.

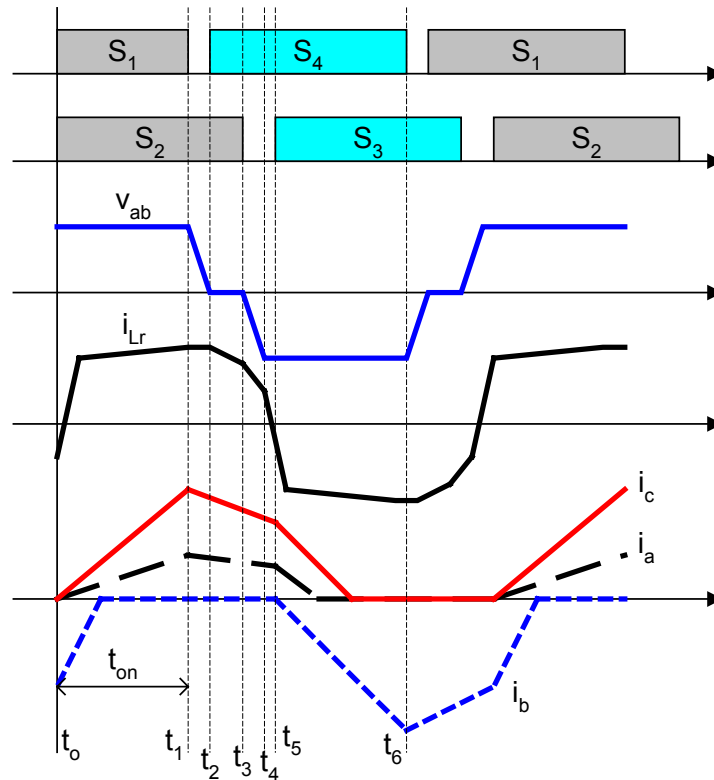


Fig. 4-3. Main waveforms.

To explain the operating stages, the components in the converter are considered ideal, the intermediate bus capacitors are constant voltage sources, and the AC input voltages are constant within one switching cycle. The capacitors C_a , C_b and C_c and the input filter will be ignored for simplicity of explanation. To achieve low harmonic distortion in the input currents, the boost inductors must operate in DCM. Nevertheless, the DC side of the three-level converter may be operated either in CCM or DCM. In the description that follows, only CCM operation is considered for the DC side of the three-level structure.

The proposed AC/DC converter is controlled by conventional phase-shift control. All switches operate with nearly 50% duty cycle, while a dead time is required to avoid shoot-through of the power switches. As can be seen in the diagram shown in Fig. 4-2(c), the outer switches S_1 and S_4 are 180° apart. The inner switches S_2 and S_3 are also complementary, while phase-shifting the

outer switches with respect to the inner switches controls the DC output voltage. Compared with the modulation strategy applied to the conventional full-bridge phase-shift converter [77] [78], the leading leg in the three-level structure is associated with the outer switches, while the lagging leg is associated with the inner switches.

Stage 1 (t_0, t_1), Fig. 4-4(a): During this stage, the switches S_1 and S_2 are turned on. The currents i_a and i_c rise linearly while i_b decreases, as illustrated by the waveforms in Fig. 4-3. Power is delivered to the output, and the current i_b is completely reset.

Stage 2 (t_1, t_2), Fig. 4-4(b): At instant t_1 , S_1 is turned off and C_1 is charged towards the voltage across the capacitor C_{b1} . Simultaneously, C_4 is discharged towards zero through the clamping capacitor C_f . This stage ends when the diode D_{c1} clamps the voltage across the capacitance C_1 to the voltage across C_{b1} . At the same time, the voltage across C_4 reaches zero.

Stage 3 (t_2, t_3), Fig. 4-4(c): This is the freewheeling stage of the output current that starts when the voltage across C_1 reaches the voltage across C_{b1} , turning on the diode D_{c1} . The input currents i_a and i_c decrease during this interval.

Stage 4 (t_3, t_4), Fig. 4-4(d): At instant t_3 , S_2 is turned off and the resonant inductance placed in the primary side for the purpose of soft switching resonates with the capacitances C_2 and C_3 . The voltage across C_2 rises to half of the intermediate bus voltage, while the voltage across C_3 decreases to zero to complete the stage. The currents i_a and i_c continue decreasing during this stage.

Stage 5 (t_4, t_5), Fig. 4-4(e): During this interval, the anti-parallel diodes of S_3 and S_4 conduct both the primary current of the transformer and the remaining levels of input AC currents. The current in phase b starts building up because the conduction of the intrinsic diodes of S_3 and S_4

short out the inductor L_b across voltage v_b . The switches S_3 and S_4 can then be turned on at zero-voltage condition during this stage.

Stage 6 (t_5, t_6), Fig. 4-4(f): During this stage, S_3 and S_4 are turned on. Currents through L_a and L_c decrease to zero, and the current through L_b increases linearly. Power is delivered to the output side during this interval. After instant t_6 , another half operating cycle will be repeated for switches S_3 and S_4 .

4.3.2. Analysis of the TL-PS AC/DC Converter

This section analyzes the operation of the proposed converter to devise design guidelines. The discussion is divided in two parts: (1) AC-side and (2) DC-side analyses. According to the operating stages, the boost inductor currents are independent from each other because the neutral point is connected to the switching power stage. As a result, the analysis performed in one phase can be extended to the remaining phases.

A. AC-Side Analysis

For this analysis, the three-phase input voltages are balanced, while the voltage across phase a is taken as the reference voltage for the three-phase system. A conceptual representation of the current in the boost inductor connected to phase a is shown in Fig. 4-5 for half of a line cycle. During the intervals $0 < \theta < \phi_{cr}$ and $(\pi - \phi_{cr}) < \theta < \pi$, the boost inductor current in phase a is completely reset during the freewheeling stage (stage 3 shown in Fig. 4-4(c)). However, for the remaining interval $\phi_{cr} < \theta < (\pi - \phi_{cr})$ of the half-line cycle, the time duration of the freewheeling interval is not sufficient to completely reset the boost inductor current in phase a. This is the reason why the boost current waveforms assume different slopes in the illustration shown in Fig. 4-5.

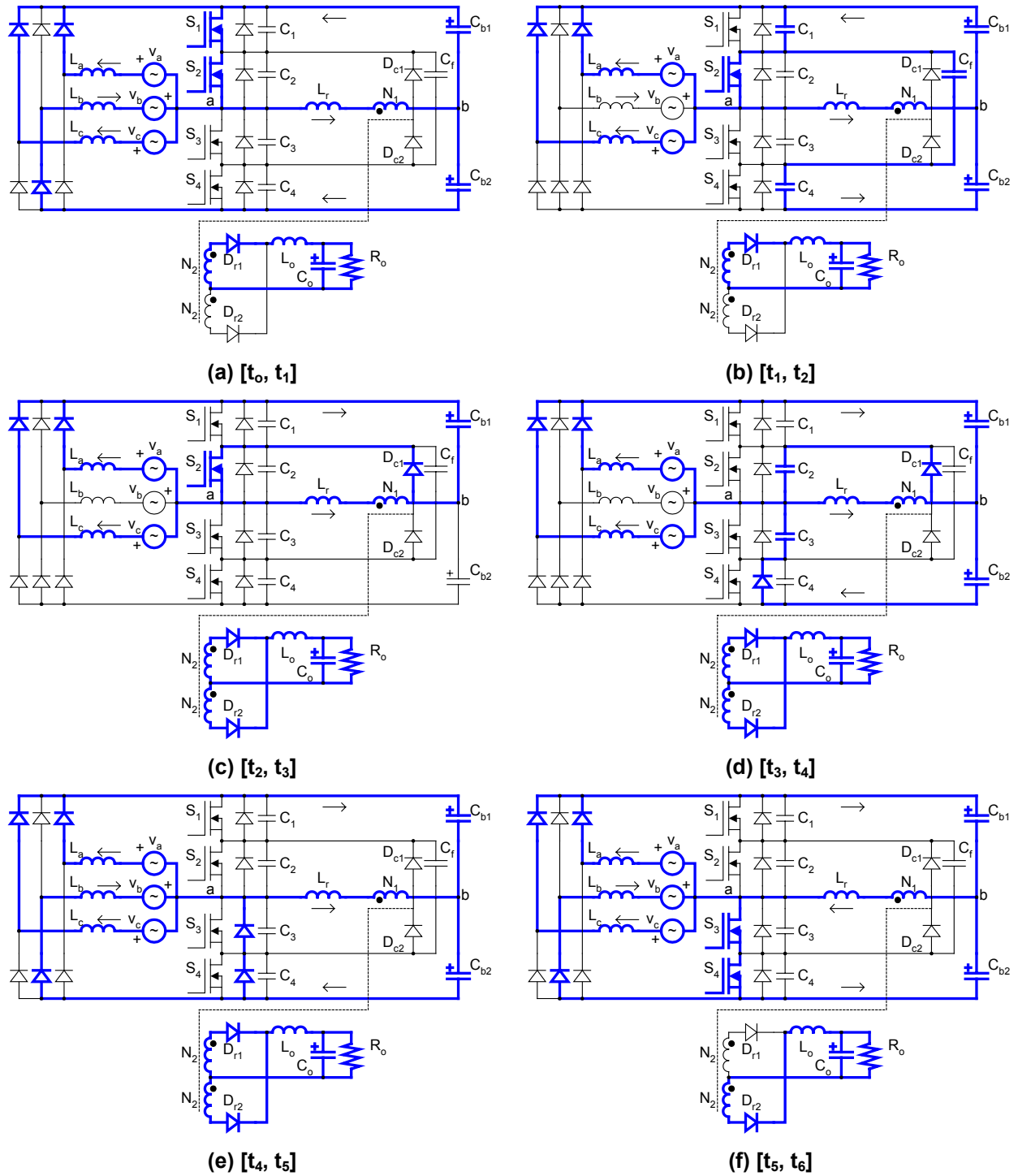


Fig. 4-4. Equivalent circuits assumed during the operating stages.

The critical angle ϕ_{cr} in which the current in phase a is completely reset during the freewheeling interval is given by

$$(4-1) \quad \phi_{cr} = \arcsin \left[\frac{V_{bus} (1 - 2D)}{2V_{pk}} \right],$$

where V_{bus} is the total intermediate bus voltage (sum of the voltages across C_{b1} and C_{b2}), V_{pk} is the peak line-to-neutral input voltage, and D is the operating duty cycle.

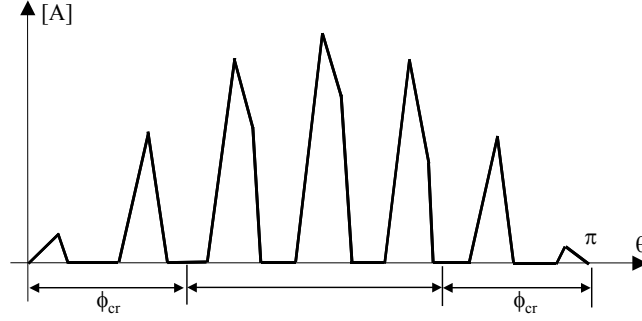


Fig. 4-5. Illustration of the boost inductor current waveform for half of a line period.

The average input phase current is obtained from the high-frequency waveform schematically shown in Fig. 4-5. For the intervals $0 < \theta < \phi_{cr}$ and $(\pi - \phi_{cr}) < \theta < \pi$, the average input current is given by

$$(4-2) \quad i_{in1}(\theta) = D^2 \frac{V_{bus} \sin(\theta)}{2 \left(\frac{V_{bus}}{V_{pk}} - 2 \sin(\theta) \right) L f_s},$$

where L is the boost inductance and f_s is the switching frequency.

During the remaining interval $\phi_{cr} < \theta < (\pi - \phi_{cr})$, the average input current is given by

$$(4-3) \quad i_{in2}(\theta) = V_{bus} \frac{2V_{pk} (4D^2 + 1) \sin(\theta) - V_{bus} (2D - 1)^2}{32 (V_{bus} - V_{pk} \sin(\theta)) L f_s}.$$

After obtaining the average input current for all the sub-intervals, the input power required from the power system and transferred to the output can be determined by

$$(4-4) \quad P = \frac{3}{\pi/2} \left[\int_0^{\phi_{cr}} V_{pk} \sin(\theta) i_{in1}(\theta) d\theta + \int_{\phi_{cr}}^{\pi/2} V_{pk} \sin(\theta) i_{in2}(\theta) d\theta \right].$$

The minimum bus voltage condition for proper operation of the proposed converter can be easily derived from the freewheeling stage shown in Fig. 4-4(c). As can be verified from that figure, at the peak voltage across phase a, the total intermediate bus voltage must be $V_{bus} \geq 2V_{pk}$ in order to provide reset voltage for the input current during the freewheeling stage (the reset mentioned here is partial and does not necessarily need to bring the boost inductor current to zero). For the polarity of the input voltages assumed in Fig. 4-4, when the total reset of the boost inductor current flowing through phase a is not achieved during the freewheeling stage, it must then be finalized during the conduction time of the switches S_3 and S_4 .

Fig. 4-6 shows the normalized intermediate bus voltage as a function of the output power. As can be seen, the PFC section of the proposed converter behaves as a current source, since the input inductors operate in DCM. The minimum intermediate bus voltage is twice the input peak line-to-neutral voltage, while the normalized variables are defined as follows:

$$(4-5) \quad M = \frac{V_{bus}}{V_{pk}}$$

$$P_{norm} = \frac{P_o L f_s}{V_{pk}^2}$$

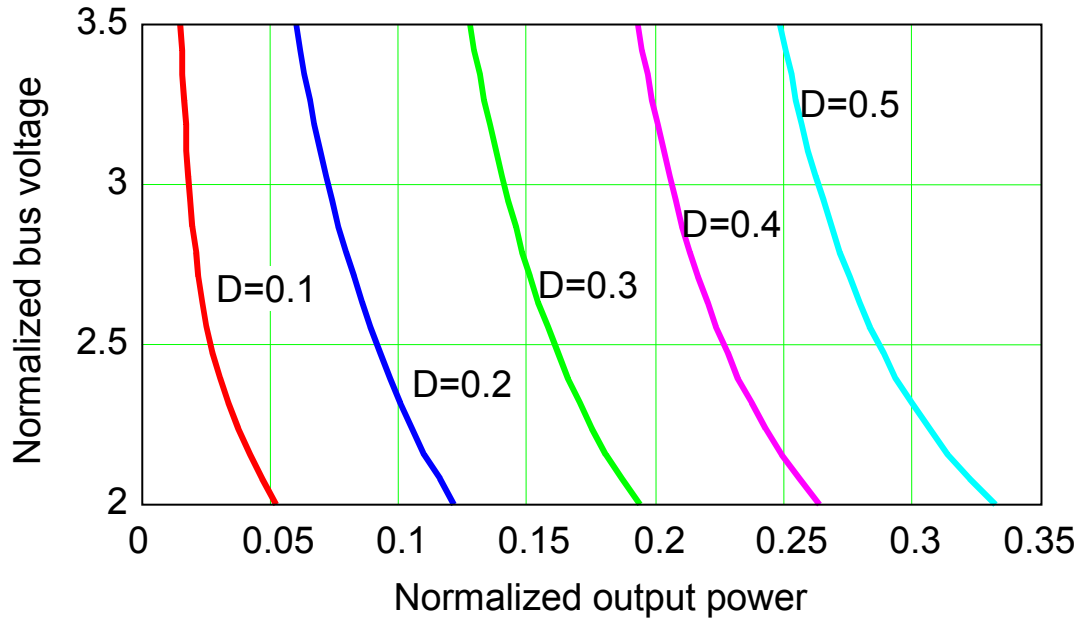


Fig. 4-6. Normalized bus voltage gain.

B. DC-Side Analysis

Depending on the output load condition, the DC side of the proposed converter operates either in DCM or CCM. For CCM operation, the output voltage is given by

$$(4-6) \quad V_o = \frac{D}{n_t} V_{bus} - \frac{4}{n_t^2} I_o L_r f_s,$$

where n_t is the transformer turns ratio, I_o is the output load current, and L_r is the total resonant inductance connected in series with the primary side of the transformer to provide energy for soft switching. Equation (4-6) shows that L_r reduces the output voltage according to the load current. The second term in (4-6) is a factor common to all converters that rely on the energy stored in the resonant inductor to achieve soft switching for the lagging switches [13].

When the output inductor of the DC side operates in DCM, the output voltage is given by

$$(4-7) \quad V_o = \frac{(DV_{bus})^2}{2n_t^2 \left[2I_o f_s \left(L_o + \frac{L_r}{n_t^2} \right) + \frac{D^2 V_{bus}}{n_t^2} \right]}$$

The results of the DC-side analysis are plotted in Fig. 4-7. The boundary line between DCM and CCM shown in Fig. 4-7 is associated with the operating mode of the output inductor. As can be observed in the CCM region, there is a drop in the output voltage caused by the resonant inductance L_r . As the resonant inductance becomes larger, the circulating energy and the output voltage drop also increase in the proposed converter. The normalized variables used to plot the curves in Fig. 4-7 are defined as follows:

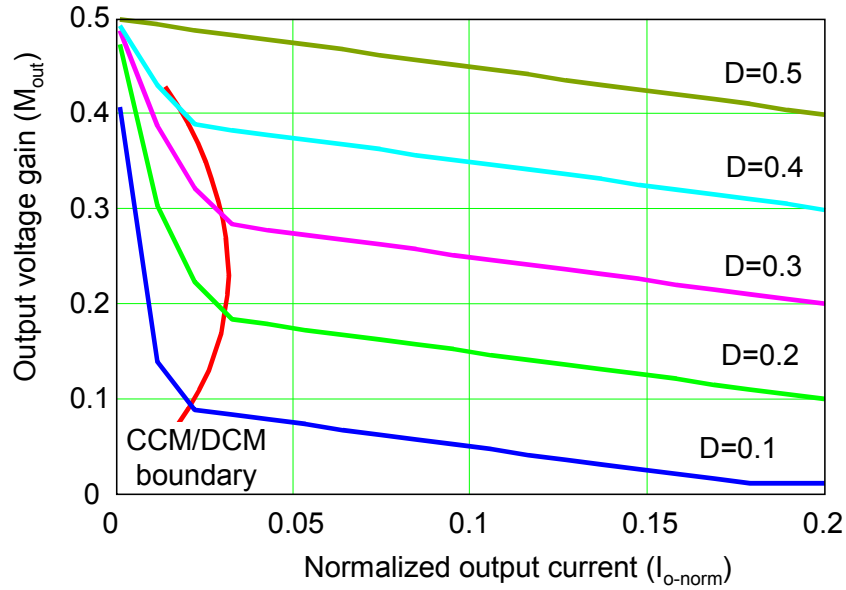


Fig. 4-7. Normalized DC output voltage as a function of normalized DC output current.

$$(4-8) \quad M_{out} = \frac{n_t V_o}{V_{bus}}$$

$$I_{o-norm} = I_o \frac{n_t L_o f_s}{V_{bus}}$$

where L_o is the output filter inductance. The curves shown in Fig. 4-7 were obtained for an inductance ratio $n_t^2 L_o / L_r = 8$. As the inductance ratio increases, the region in which the output section of the converter operates in CCM also increases. However, a larger CCM operating range in the output section of the proposed converter will increase the intermediate bus voltage, as discussed later in this chapter.

4.3.3. Design Guidelines and Example

This section describes a simplified design procedure based on the theoretical analysis presented in the previous section and provides a design example.

A. Specifications

The proposed single-stage TL-PS converter is designed to operate with an input line-to-neutral voltage of 170V to 265V RMS, 3kW of output power, and 48V of DC output voltage while operated at 100kHz of switching frequency.

B. Choosing the Design Point

To optimize the design of the proposed converter, the AC side must operate as close as possible to the DCM/CCM boundary condition, which is associated with the minimum intermediate bus voltage gain $M=2$. As already described, for proper operation of the proposed converter, the intermediate bus voltage must be two times greater than the peak input phase voltage. Under such an assumption, if the bus voltage gain (V_{bus}/V_{pk}) is set to 2.1, the input currents will be forced to operate in DCM. Choosing a minimum voltage gain of 2.1, the intermediate bus voltage will be 504V at low-line input phase voltage (170V) and full load.

C. *Duty Cycle*

The duty cycle is chosen to provide output voltage regulation at full load and low-line input voltage. The maximum duty cycle D is chosen to be 0.45, thus providing compensation for the dead time between the gate signals of the power switches. Choosing a large duty also increases the transformer turns ratio to improve converter efficiency.

D. *Boost Inductance*

The power delivered to the output is limited by the boost inductances. According to (4-4) and the results from the previous analysis, the power delivered to the output can be represented as a function of the following parameters:

$$(4-9) \quad P = f(V_{bus}, V_{pk}, D, L, f_s).$$

At low-line input voltage and full-load condition, all parameters in (4-9) are known, except that the boost inductance must be determined. Solving (4-4) for the boost inductance and taking into account the design point already established above (170V of input phase voltage, 504V of intermediate bus voltage, 0.45 of duty cycle, and 100kHz of switching frequency), the resulting boost inductance is 55 μ H. If the proposed converter is to operate at a different switching frequency, then the curve shown in Fig. 4-8 should be used.

E. *Transformer Turns Ratio*

The output voltage given in (4-6) can be rewritten as follows:

$$(4-10) \quad \frac{n_t V_o}{V_{bus}} = D - \frac{4 I_o L_r f_s}{n_t V_{bus}}$$

The second term in (4-10) is the well-known duty-cycle loss. Increasing this term means obtaining ZVS at lighter loads. However, increasing the duty-cycle loss also increases the circulating energy in the converter. Choosing a duty-cycle loss equal to 0.07 yields $n_t=4$.

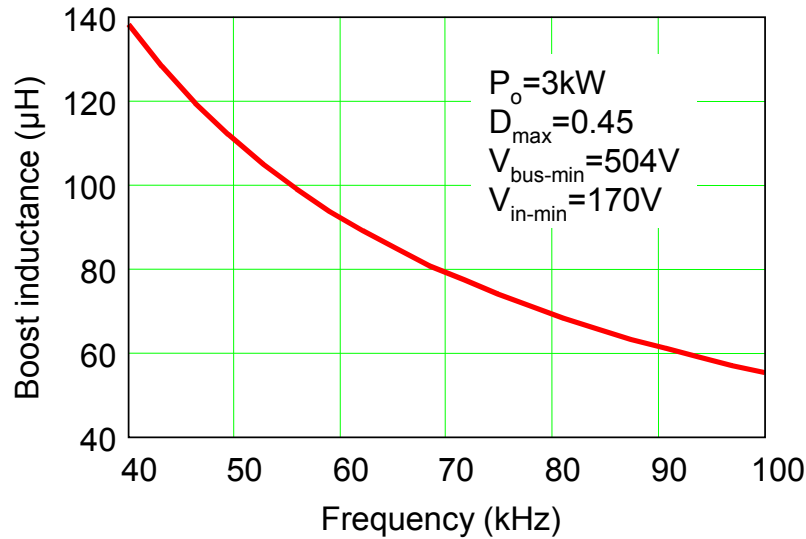


Fig. 4-8. Boost inductance as a function of the switching frequency for DCM operation.

F. Resonant and Output Filter Inductance

The resonant inductance is obtained from the duty-cycle loss term defined in (4-10), as follows:

$$(4-11) \quad L_r = \frac{n_t D_{loss} V_{bus}}{4 I_o f_s}$$

In this case, the full-load output current is considered in the calculation in order to guarantee regulation of the output voltage. Substituting all pertinent values into (4-11), the resonant

inductance is $L_r=5.65\mu\text{H}$. From the assumption taken before that $n_t^2 L_o/L_r = 8$, the output filter inductance is $2.83\mu\text{H}$.

The impact of the inductance ratio on the maximum intermediate bus voltage is shown in Fig. 4-9. As can be seen, the intermediate bus voltage increases with the inductance ratio. The inductance ratio, $n_t^2 L_o/L_r$, influences the current ripple in the output inductor, or more specifically, influences the extent to which the output section is designed to operate in CCM. As the inductance ratio increases, the region in which the output inductor operates in CCM also increases, and so does the maximum intermediate bus voltage.

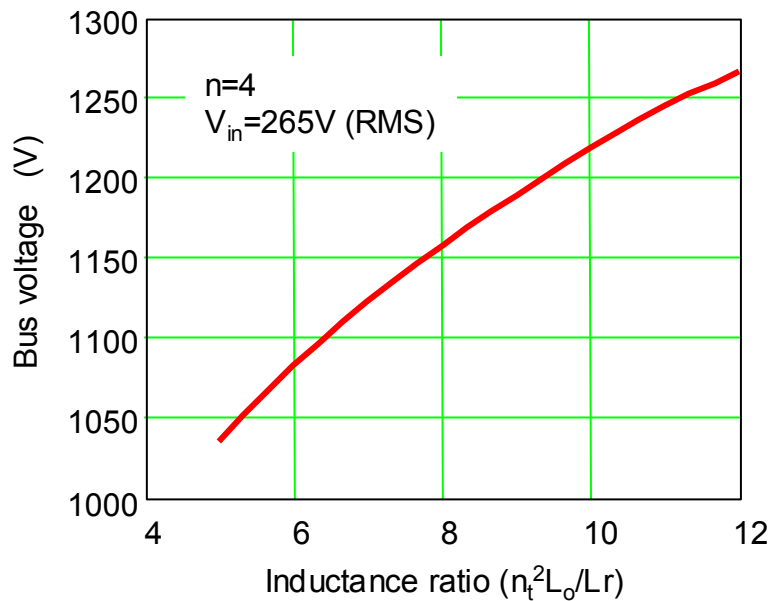


Fig. 4-9. Calculated maximum intermediate bus voltage stress as a function of inductance ratio.

4.3.4. Harmonic Distortion of the Input Current

To obtain the THD of the proposed converter, the Fourier analysis can be applied to the instantaneous average boost inductor current given in (4-2) and (4-3). It is important to mention that the instantaneous average boost inductor current given in (4-2) and (4-3) includes the zero-

sequence-order harmonics, since the neutral point connection was used in the analytical model. As a result, a third harmonic circulates in the power lines. However, as mentioned before, the AC capacitors are used to provide an artificial neutral point connection in order to eliminate the circulation of the zero-sequence-order harmonics from the input lines.

The THD of the instantaneous average boost inductor current, including the third harmonic, is plotted in Fig. 4-10(a). As can be verified, the distortion is high when the third harmonic is not eliminated from the line current. However, Fig. 4-10(b) shows that the distortion is very low when the zero-sequence-order harmonics are eliminated from the power source by using the artificial neutral point connection created by the AC capacitors. As shown in Fig. 4-10, the THD of the input line currents depends upon the duty cycle. This result makes sense because when the duty cycle increases, the freewheeling time is reduced, and consequently the faster slope of the reset seen in Fig. 4-3 dominates the reset of the boost inductors, thus reducing the THD. Fig. 4-10(b) shows a comparison between the THD produced by the proposed converter and that generated by the three-phase single-switch DCM boost rectifier [42]. For the same intermediate bus and input voltages, the THD generated by the proposed converter is much lower than that which is generated by the three-phase single-switch DCM boost rectifier (observe that a log scale was used to plot the THD without the zero-sequence order harmonics).

4.3.5. Experimental Results

This section presents the experimental results obtained from the proposed TL-PS AC/DC converter. The implemented switching power stage used IXFN44N80 MOSFETs, RUR30120 line rectifiers and clamping diodes, and HFA120MD40D output rectifiers. Each bus capacitance

consisted of three $1000\mu\text{F}/250\text{V}$ electrolytic capacitors connected in series, while the clamping capacitor C_f and the AC capacitors C_a , C_b and C_c were implemented with $2\mu\text{F}$ polypropylene-type capacitors. The output filter inductance was $3\mu\text{H}$, while the output filter capacitor was $2 \times 4700\mu\text{F}/100\text{V}$.

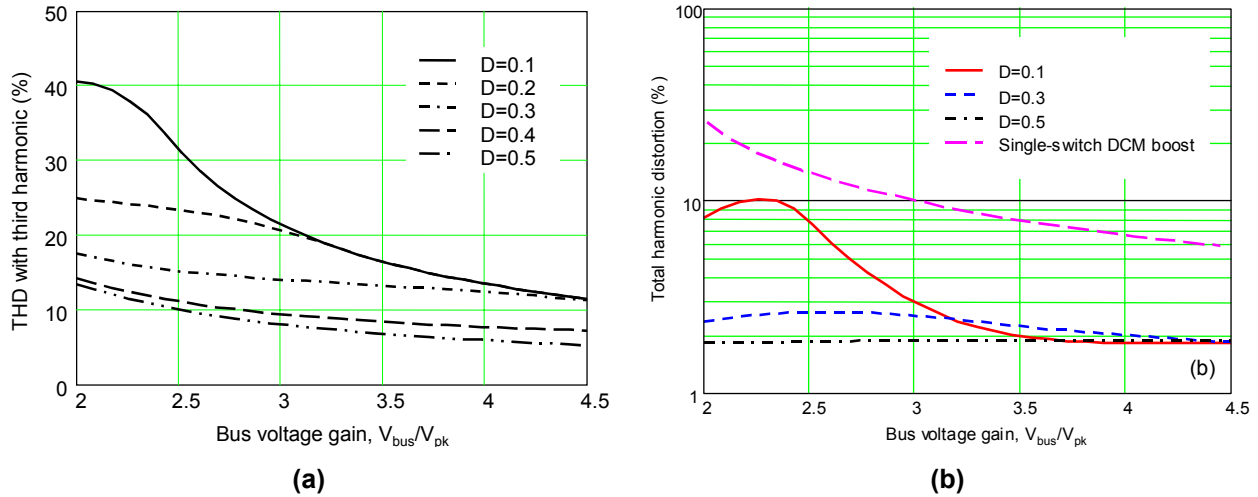


Fig. 4-10. THD: (a) with third harmonic, and (b) without third harmonic.

Fig. 4-11(a) shows the measured input phase voltage and the input current of the proposed converter at full load. The THD of the current waveform illustrated in Fig. 4-11(a) is only 4.8%. The fifth harmonic is still dominant in the input current, accounting for an individual distortion of 4.3%. Fig. 4-11(b) shows the voltage v_{ab} and the primary transformer current as indicated in Fig. 4-2(b). These waveforms are similar to the classic waveforms produced by the DC/DC converters with phase-shift control and ZVS operation. Fig. 4-11(c) shows the voltages and currents through switches S_2 (inner switch) and S_4 (outer switch). As can be seen, the outer and inner switches operate with zero-voltage turn-on.

The intermediate bus voltage measured at three different input voltages is shown in Fig. 4-12(a). The bus voltage depends on the input voltage as well as on the output load variations. For a

given input voltage, the intermediate bus voltage increases as the load decreases. However, there is a region in the plots where the intermediate bus voltage remains approximately constant. In that region, the DC side of the proposed converter starts operating in DCM. This operating mode helps to limit the increase of the bus voltage. Therefore, by reducing the output inductance, the power level at which the DC side starts operating in DCM decreases and the intermediate bus is limited to lower voltages. However, reducing the output inductance incurs more current stress in the primary switches and more current ripple in the output section. According to Fig. 4-9, reducing the output inductance is equivalent to reducing the inductance ratio $n_t^2 L_o/L_r$, which results in decreasing the maximum intermediate bus voltage stress.

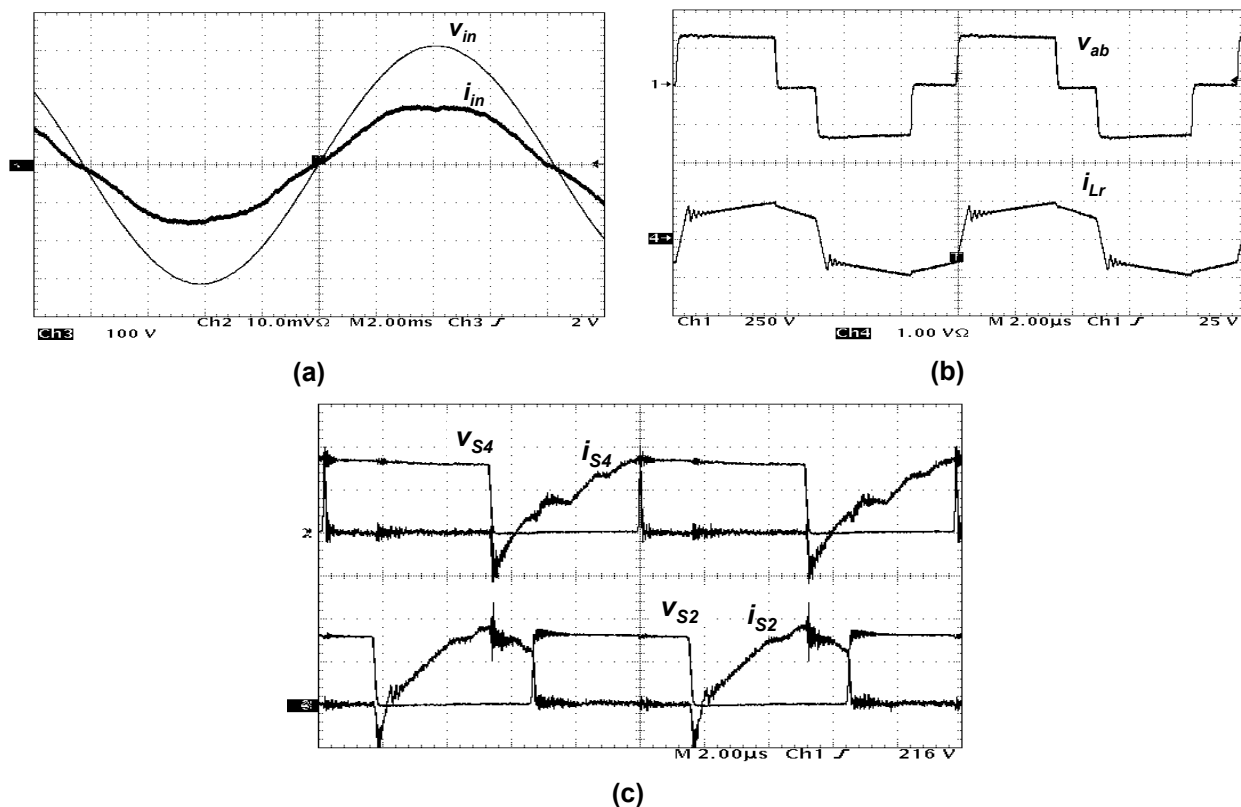


Fig. 4-11. Experimental waveforms: (a) input voltage (100V/div) and filtered input current (5A/div), (b) voltage v_{ab} (250V/div) and primary current (10A/div), and (c) ZVS waveforms (voltages: 200V/div and currents: 20A/div).

Fig. 4-12(b) shows the measured THD versus the output load for three different input voltages. The harmonic distortion is always lower than 9%, even at high-line input voltage. It is also noteworthy that the experimental THD is higher than the theoretical distortion shown in Fig. 4-10(b). The reason for this difference can be attributed to the fact that the AC capacitors used to provide the artificial neutral connection do not result in ideal voltage sources (designed as those that are free of harmonics), and consequently the THD of the input currents is higher than that obtained from the theoretical analysis.

The measured converter efficiency at full load, 100kHz, and 220V input line-to-neutral voltage is shown in Fig. 4-12(c). Despite the ZVS operation provided by the converter, the efficiency is rather low for the power level under discussion. The main reason for the low efficiency is the high input current ripple that occurs due to the DCM operation of the boost inductors. The circulating energy that is seen in the current waveform i_{Lr} and the turn-off loss of the power switches also contribute to the reduction in converter efficiency.

A solution for reducing the switching loss is to decrease the switching frequency. Fig. 4-12(c) shows the improvement in efficiency gained by cutting back the switching frequency to 50kHz. At 50kHz, the converter parameters are $L=110\mu\text{H}$, $L_r=11.3\mu\text{H}$, and $L_o=5.7\mu\text{H}$. All the power devices were the same as those used for the design at 100kHz in order to retain the same level of conduction loss in the circuit. As can be verified, the efficiency at 50kHz is significantly improved, which proves that the turn-off loss plays an important role in converter efficiency. The turn-off loss is rather high because the switches carry both the boost inductor currents from the AC side and the DC output current reflected to the primary side of the transformer.

Consequently, there is a high level of current flowing through the power switches during turn-off, which contributes to the increase in turn-off loss.

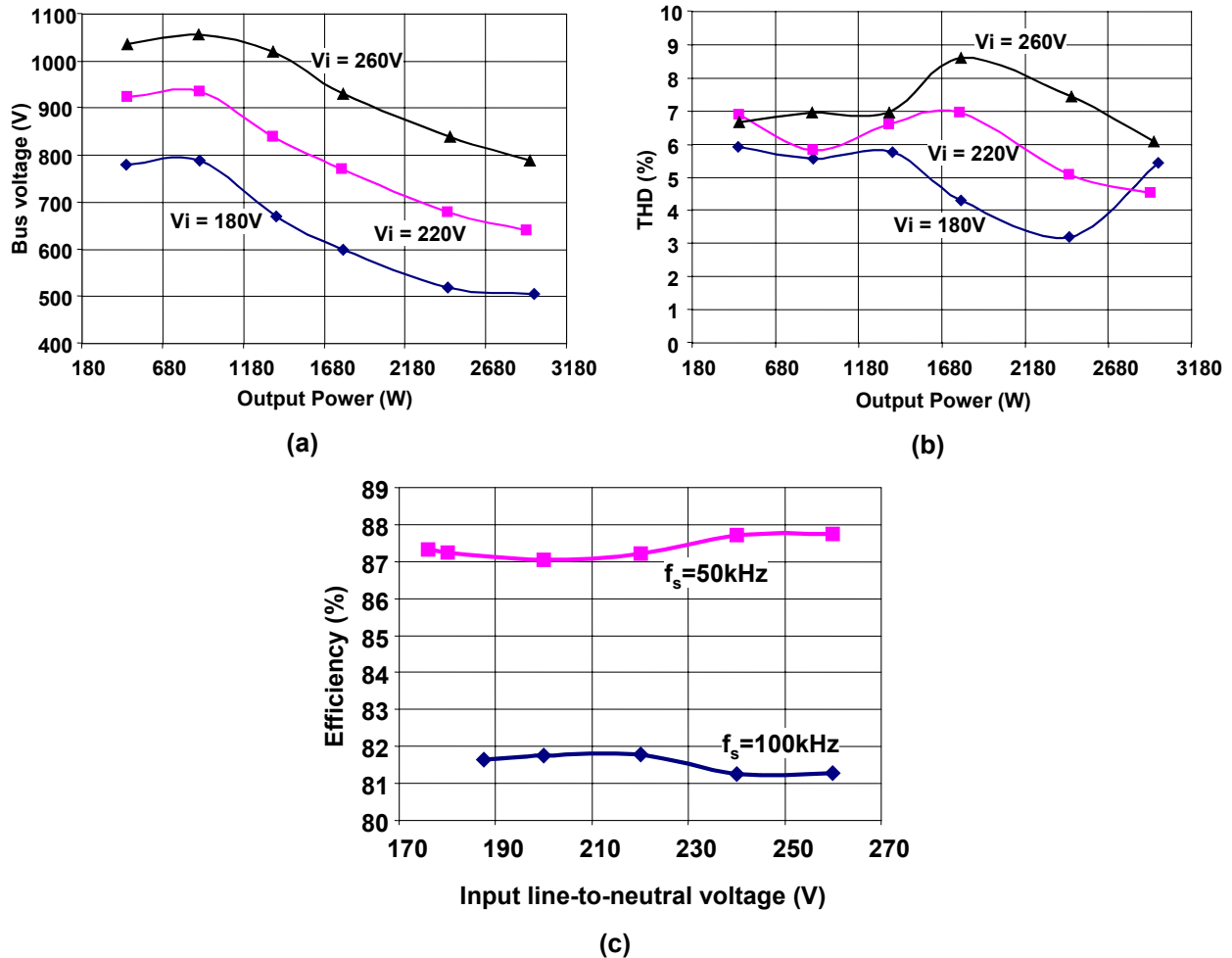


Fig. 4-12. Experimental results: (a) intermediate bus voltage, (b) THD, and (c) converter efficiency measured for both designs.

The reason for the reduced efficiency of the TL-PS single-stage AC/DC converter can be better understood by referring to Fig. 4-13. In order to transfer power to the output and to store energy in the input inductors, either the upper or the lower switches must be on. As can be seen, the rectified input currents flow through both switches at the same time, which increases the circuit conduction loss. Moreover, since the input currents are discontinuous, the switches are turned off at the peak of the rectifier input currents during every switching cycle, thus increasing the

switching loss. The next section of this chapter presents a topological variation of the single-stage AC/DC converter that is used to reduce conduction loss.

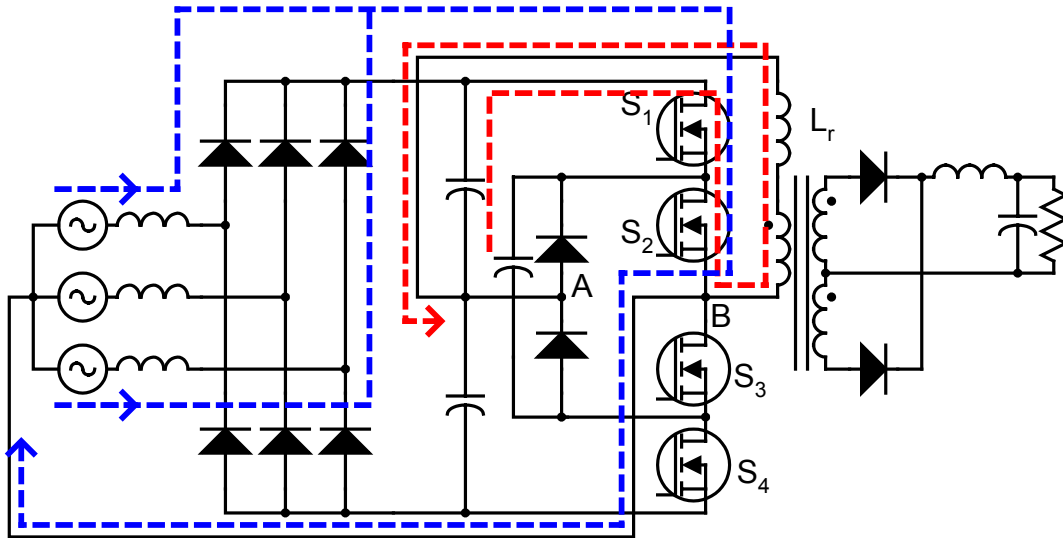


Fig. 4-13. Main current path through the power switches.

4.4. Single-Stage Three-Level Asymmetrical (TL-AS) Front-End Converter

The three-level DC/DC converter depicted in Fig. 4-1 was based on the neutral-point-clamped (NPC) three-level inverter [79], which also served as the starting point for the single-stage TL-PS AC/DC converter discussed in the previous section. However, other multilevel topologies can also be used to realize different three-level DC/DC converters [80]-[82]. For instance, one topological variation for the DC/DC converter is illustrated in Fig. 4-14(a). This topology uses stacked switches to achieve a multi-level arrangement that is simpler than the NPC structure. The control of the converter illustrated in Fig. 4-14(a) is based on the asymmetrical PWM control, leading to the waveforms shown in Fig. 4-14(b).

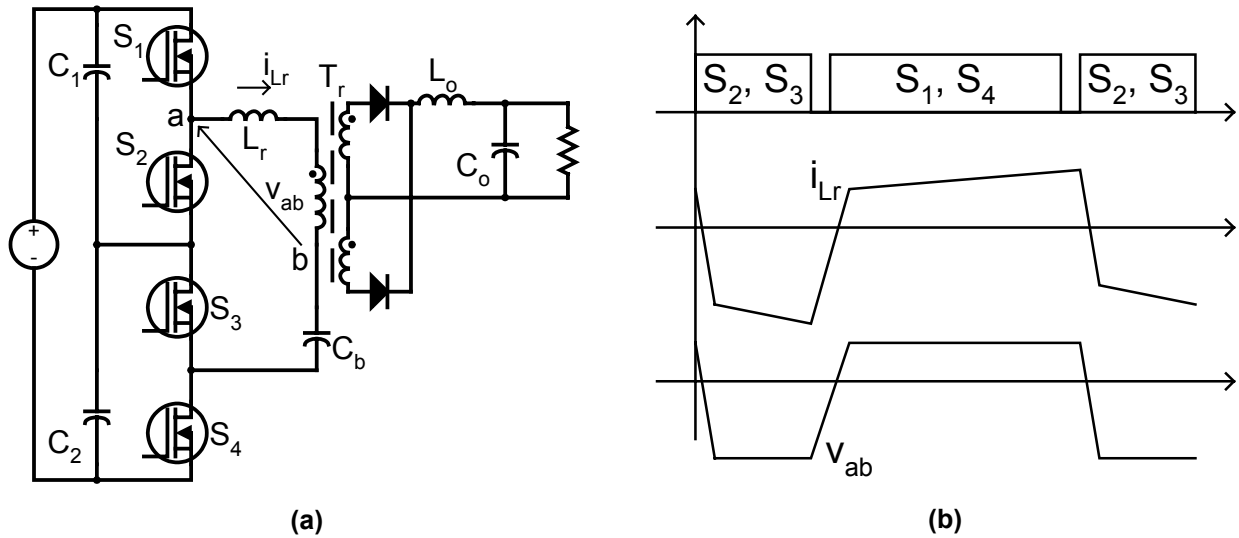


Fig. 4-14. Three-level asymmetrical DC/DC converter: (a) topology and (b) waveforms.

The topology shown in Fig. 4-14(a) can easily be combined with a rectifier bridge to form an AC/DC converter similar to the one described in the previous section of this chapter. The starting point is the two-stage front-end converter based on the two-switch three-level DCM boost rectifier, followed by an asymmetrical PWM three-level DC/DC converter, as shown in Fig. 4-15(a). The synthesis of the single-stage converter is obtained by removing the switches and diodes of the PFC stage, while connecting the positive and negative outputs of the bridge rectifier as shown in Fig. 4-15(b).

4.4.1. Circuit Description and Operation

In the proposed circuit, the four switches are connected in a stacked three-level structure, while an asymmetrical PWM is used to control the DC output voltage. The capacitor C_b is used to provide voltage balance across the transformer because of the asymmetrical duty ratio imposed by the control. The current source in parallel with the transformer is fictitious and represents the DC bias of the magnetizing current caused by the asymmetrical PWM. The resonant inductance

L_r is connected in series with the transformer in order to increase the ZVS operating region for the proposed converter. The input boost inductors must operate in DCM to guarantee low THD for the input currents, while the AC capacitors are incorporated by the input filter and provide an artificial neutral connection point for the switching power stage. The bus capacitors C_1 and C_2 provide energy storage as well as resetting voltage to the input boost inductors. Either the inner or outer switches are turned on and off simultaneously in order to transfer power to the output section. The following paragraphs describe the operating stages of the proposed converter.

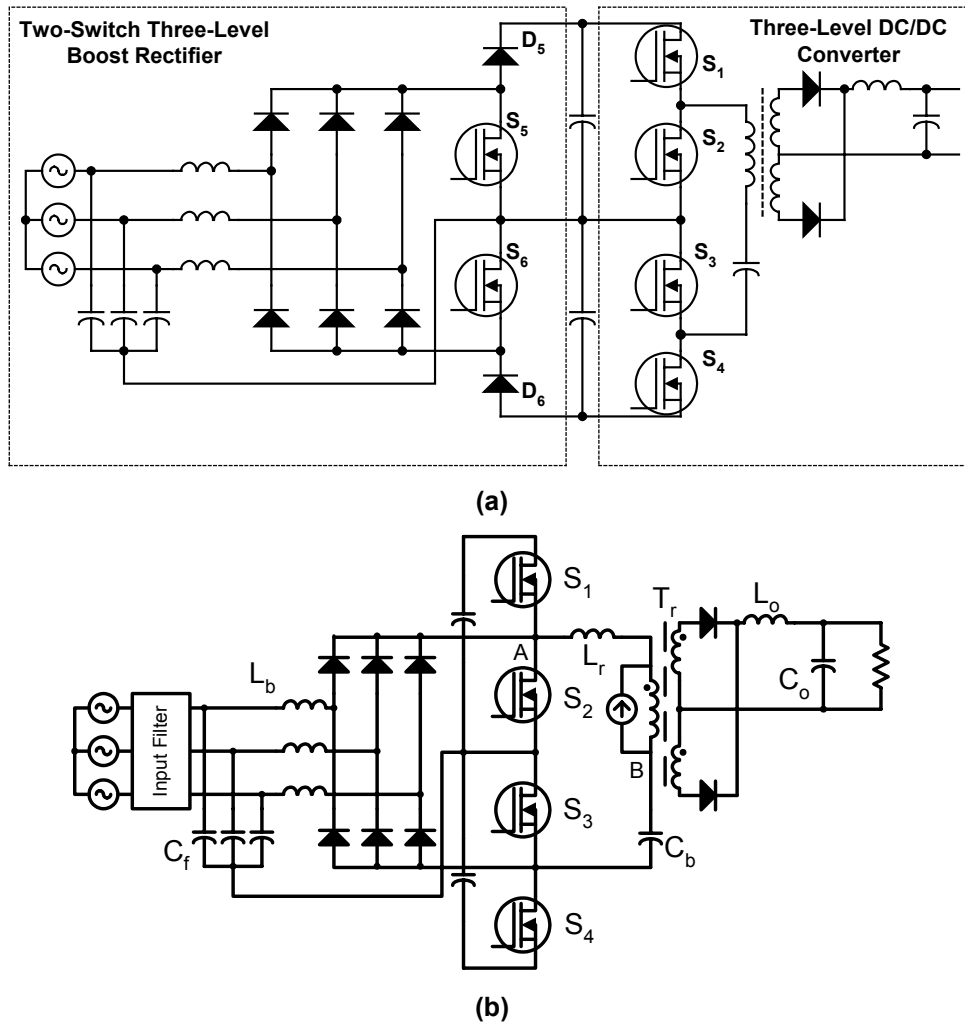


Fig. 4-15. Synthesis process: (a) two-stage approach, and (b) TL-AS single-stage AC/DC converter.

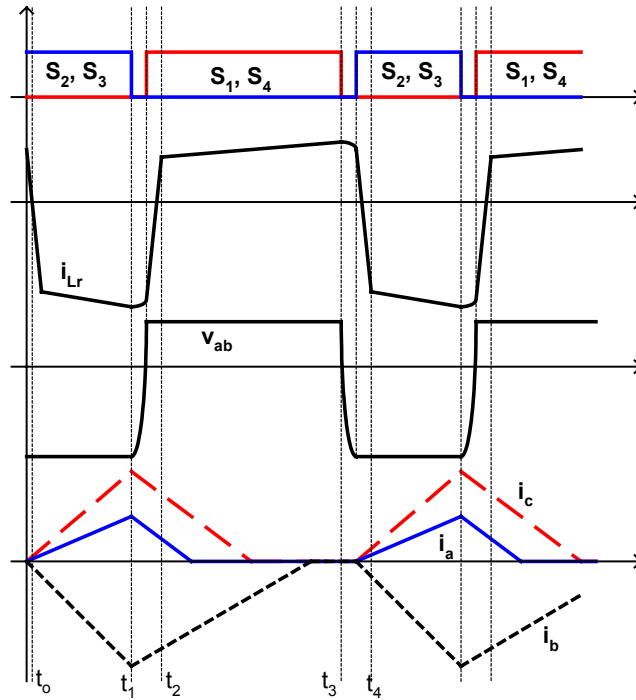


Fig. 4-16. TL-AS converter main waveforms.

Stage 1 (t_0, t_1), Fig. 4-17(a): During this stage, S_2 and S_3 are on in order to store energy in the input inductors, while the blocking capacitor is discharged across the transformer and output filter.

Stage 2 (t_1, t_2) Fig. 4-17 (b): In this stage, the switches S_2 and S_3 are turned off. The rectified boost inductor currents and the current in L_r charge the intrinsic capacitances of S_2 and S_3 , as well as discharging the capacitances of S_1 and S_4 . When the voltages across S_1 and S_4 reach zero, the rectified input currents and i_{Lr} are diverted into the intrinsic diodes of the switches S_1 and S_4 , providing the condition for zero-voltage turn-on for S_1 and S_4 . During this stage, the resonant inductor current will reverse its polarity because the total bus voltage is greater than the voltage across the DC blocking capacitor C_b . Because S_1 and S_4 operate for longer times than S_2 and S_3 , the DC bias of the transformer magnetizing current builds up according to the polarity shown in Fig. 4-17. Therefore, this stage ends when the primary current of the transformer reaches the

difference between the reflected output inductor current and the DC magnetizing current of the transformer.

Stage 3 (t_2, t_3), Fig. 4-17 (c): During this stage, power is transferred from the bus capacitors C_1 and C_2 to the output, while the input inductors are reset by the difference between half of the intermediate bus voltage and the input phase voltage source connected to the boost inductor.

Stage 4 (t_3, t_4), Fig. 4-17 (d): When the switches S_1 and S_4 are turned off, the primary current will charge the intrinsic capacitances of S_1 and S_4 , as well as discharging the capacitances of S_2 and S_3 . Once this transition has been finalized, the remaining primary current will circulate through the intrinsic diodes of S_2 and S_3 , which provides the condition for zero-voltage turn-on. During this stage, the primary current will reverse its polarity until it reaches the sum of the reflected output current and the DC magnetizing current. Once this condition has been reached, the converter will initiate another operating cycle.

This circuit variation can reduce the conduction loss because the input currents, after being rectified, circulate through only one switch at a time, as opposed to the circuit discussed in the previous section.

4.4.2. Analysis of the TL-PS AC/DC Converter

This section provides the analytical results obtained from the proposed topological variation. The discussion is also divided into AC-side and DC-side analyses. The neutral point connected to the switching power stage decouples the input phase currents from each other. As a result, the analysis performed for one phase can be extended to the other phases as well.

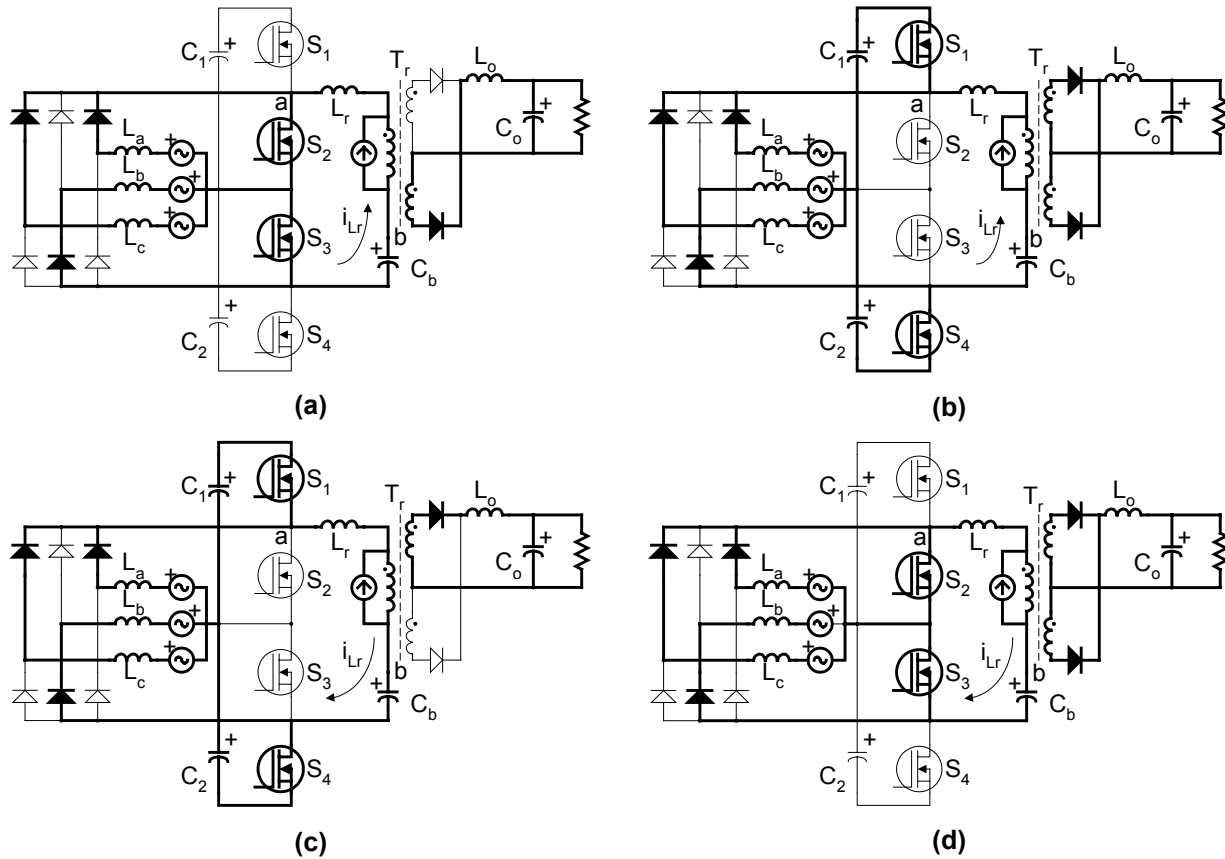


Fig. 4-17. Operating stages.

A. AC-Side Analysis

For this analysis, the three-phase input voltages are considered balanced voltages, while the voltage across phase a is used as the reference voltage. The peak boost inductor currents can be determined according to the following matrix equation:

$$(4-12) \quad \begin{bmatrix} I_{a-pk} \\ I_{b-pk} \\ I_{c-pk} \end{bmatrix} = \begin{bmatrix} \frac{D}{Lf_s} & 0 & 0 \\ 0 & \frac{D}{Lf_s} & 0 \\ 0 & 0 & \frac{D}{Lf_s} \end{bmatrix} \begin{bmatrix} v_a \\ v_b \\ v_c \end{bmatrix},$$

where v_a , v_b and v_c are the three-phase input voltages given by (2-1) (see page 21).

The time needed to reset each boost inductor depends upon the difference between half of the total intermediate bus voltage and the instantaneous input phase voltage applied across the boost inductor. For each of the input phases, the time needed to reset the boost inductor is

$$(4-13) \quad \begin{bmatrix} t_{da} \\ t_{db} \\ t_{dc} \end{bmatrix} = \begin{bmatrix} \frac{2V_{pk} \sin(\theta) \frac{D}{(V_{bus} - 2V_{pk} \sin(\theta)) f_s}}{2V_{pk} \sin\left(\theta + \frac{\pi}{3}\right) \frac{D}{\left(V_{bus} - 2V_{pk} \sin\left(\theta + \frac{\pi}{3}\right)\right) f_s}} \\ \frac{2V_{pk} \cos\left(\theta + \frac{\pi}{6}\right) \frac{D}{\left(V_{bus} - 2V_{pk} \cos\left(\theta + \frac{\pi}{6}\right)\right) f_s}} \end{bmatrix} \cdot$$

After determining the peak boost inductor currents and the time needed to reset each boost inductor, the instantaneous average boost inductor currents over a half-line period can be determined as follows:

$$(4-14) \quad \begin{bmatrix} i_a \\ i_b \\ i_c \end{bmatrix} = \begin{bmatrix} \frac{D^2 V_{pk} \sin(\theta) \frac{V_{bus}}{2L f_s (V_{bus} - 2V_{pk} \sin(\theta))}}{D^2 V_{pk} \sin\left(\theta + \frac{\pi}{3}\right) \frac{V_{bus}}{2L f_s \left(-V_{bus} + 2V_{pk} \sin\left(\theta + \frac{\pi}{3}\right)\right)}} \\ \frac{D^2 V_{pk} \cos\left(\theta + \frac{\pi}{6}\right) \frac{V_{bus}}{2L f_s \left(V_{bus} - 2V_{pk} \cos\left(\theta + \frac{\pi}{6}\right)\right)}} \end{bmatrix} \cdot$$

The previous result can be used to determine the amount of power transferred to the output as a function of the circuit parameters and control variables, as follows:

$$(4-15) \quad P_{on} = \frac{3}{8} D^2 M \frac{4M^2 \left[\tan^{-1} \left(\frac{M-2}{\sqrt{M^2-4}} \right) + \tan^{-1} \left(\frac{2}{\sqrt{M^2-4}} \right) \right] - (4 + \pi M) \sqrt{M^2-4}}{\pi \sqrt{M^2-4}},$$

where

$$(4-16) \quad M = \frac{V_{bus}}{V_{pk}}, \text{ and}$$

$$(4-17) \quad P_{norm} = \frac{P_o L f_s}{V_{pk}^2}.$$

The voltage gain (V_{bus}/V_{pk}) is plotted in Fig. 4-18 as a function of the normalized output power, using D as a running parameter. Notice that because of the slope of the voltage gain, the AC side of the converter behaves as a current source.

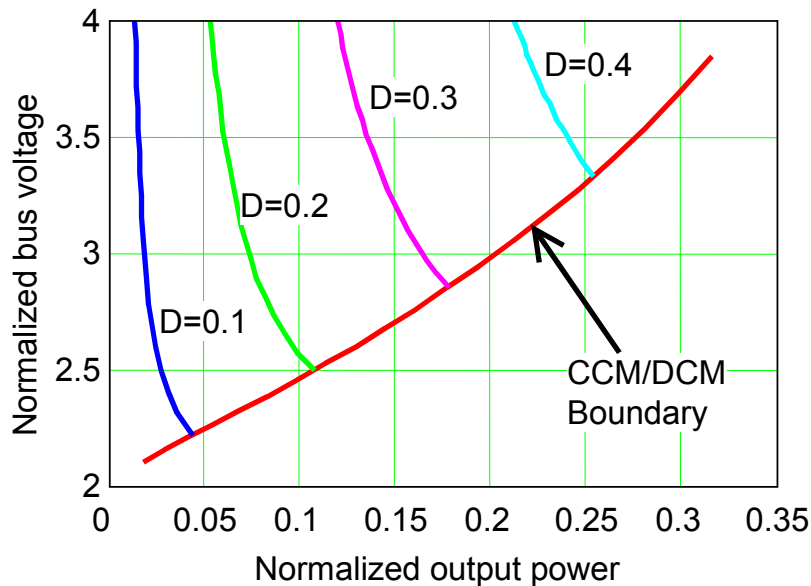


Fig. 4-18. Normalized bus voltage gain for the TL-AS AC/DC converter.

The boundary condition can be easily obtained from (4-13) by setting $t_{da}=(1-D)/f_s$ at $\theta=\pi/2$, which yields:

$$(4-18) \quad M_{cr} = \frac{2}{1-D}.$$

Therefore, to guarantee operation of the topological variation in DCM, one has to ensure that $M > M_{cr}$ for a given duty cycle.

The DC blocking capacitor is used to balance the voltage across the transformer. The voltage across C_b depends upon both duty cycle and intermediate bus voltage. The voltage ripple across C_b is controlled by its capacitance value and the amount of current that flows in the primary side. In order to balance the voltage across the transformer, the DC blocking capacitor voltage will vary according to:

$$(4-19) \quad V_c = (1-D)V_{bus}.$$

Although the DC blocking capacitor provides balance to the voltage across the transformer, the asymmetrical duty cycle operation results in an average magnetizing current through the transformer. The level of DC bias depends upon the load current and duty ratio, as shown below.

$$(4-20) \quad I_{DC-mag} = \frac{(1-2D)}{n_t} I_o.$$

B. DC-Side Analysis

The DC side of the TL-AS single-stage converter can operate either in DCM or CCM, depending upon the load. For CCM operation, the output voltage is given by

$$(4-21) \quad V_o = \frac{2D(1-D)}{n_t} V_{bus} - \frac{4}{n_t^2} I_o L_r f_s.$$

Equation (4-21) shows how the voltage drop across L_r reduces the output voltage as a function of the load current.

The output side can also operate in DCM, which requires a new set of equations to describe the output voltage. Fig. 4-19(a) shows the current waveform through L_o when the DC output operates in DCM. There are three sub-intervals during the DCM operation of the DC output side. As can be seen, these sub-intervals are associated with different equivalent circuits. For simplicity, these equivalent circuits are obtained by neglecting the magnetizing current of the transformer. The average DC output current can be determined by the following relationship:

$$(4-22) \quad I_o = \frac{1}{T_s} \left(\frac{D T_s I_{pk}}{2} + \frac{(I_{pk} + I_q) \Delta t}{2} + \frac{t_q I_q}{2} \right).$$

All the variables in (4-22) can be determined from the equivalent circuits shown in Fig. 4-19. For instance, during the magnetizing interval of L_o , switches S_2 and S_3 are on. From the circuit shown in Fig. 4-19(b), one can conclude that the peak current through inductor L_o is given by:

$$(4-23) \quad I_{pk} = (V_c - n_t V_o) \left(\frac{n_t D}{(L_r + n_t^2 L_o) f_s} \right).$$

Once the interval DT_s is finished, the switches S_2 and S_3 will be turned off. For simplicity of analysis, the transition interval needed to charge and discharge the intrinsic capacitances of the power switches will be neglected. Therefore, the circuit shown in Fig. 4-19(c) is related to the interval needed for the resonant inductor to reverse its current polarity. Meanwhile, the output

voltage V_o resets the output inductor. From the analysis, the duration of this stage and the final current through the output inductor are given as follows:

$$(4-24) \quad \begin{aligned} \Delta t &= \frac{2I_{pk} L_o L_r}{L_r V_o + n_t L_o (V_{bus} - V_c)} \\ I_q &= I_{pk} - \frac{2V_o I_{pk} L_r}{L_r V_o + n_t L_o (V_{bus} - V_c)} \end{aligned}$$

The equivalent circuit shown in Fig. 4-19(d) determines the behavior of the current in the output inductor when the current through L_r reflected to the output reaches I_q . From the circuit shown in Fig. 4-19(d), the time interval needed to finish resetting the output inductor is given by:

$$(4-25) \quad t_q = \left(L_r + n_t^2 L_o \right) \frac{I_q}{n_t (n_t V_o - V_{bus} + V_c)}$$

Equations (4-23), (4-24), (4-25) and (4-19) can be substituted into (4-22) to yield the DC output voltage. Because the resulting expression for the DC output voltage is too large to fit on the page, the result is given in terms of the variables that affect the DC output voltage. The function described in (4-26), however, can be implemented in a computer algorithm designed to calculate the characteristics of the proposed TL-AS single-stage converter.

$$(4-26) \quad V_o = g(I_o, L_o, L_r, f_s, n_t, D, V_{pk}, V_{bus})$$

4.4.3. Design Guidelines and Example

This section describes a simplified design procedure for the single-stage TL-AS converter, and provides an example based on the theoretical analysis presented in the previous section.

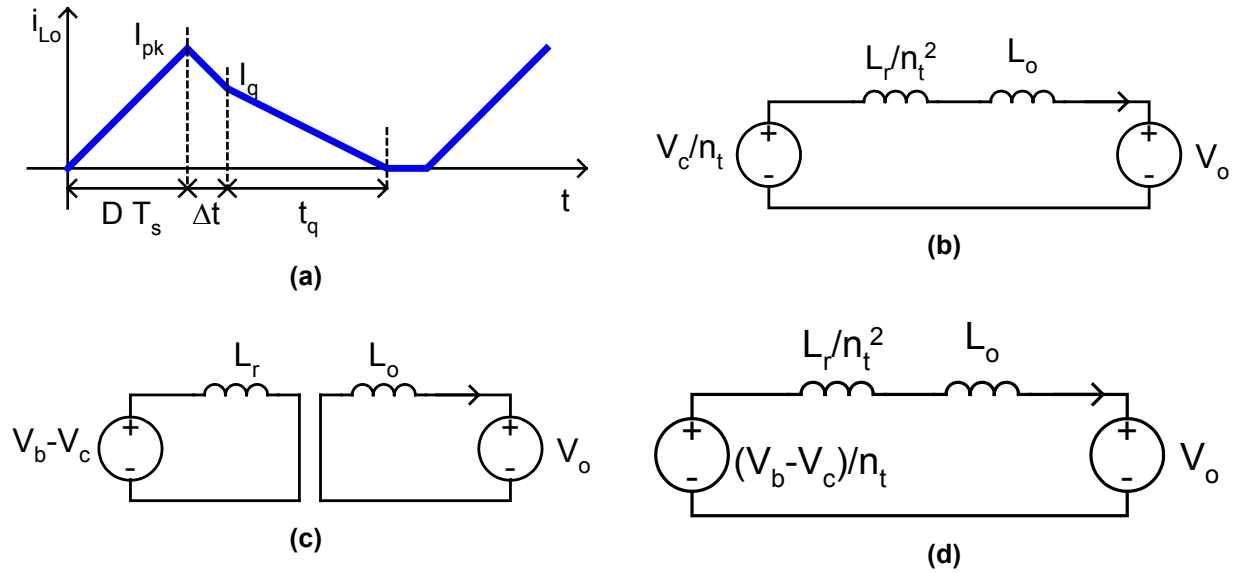


Fig. 4-19. DC-side DCM operation: (a) inductor current through L_o , (b) magnetizing stage for L_o , (c) resetting stage for L_o and reversing current polarity in L_r , and (d) final resetting stage for L_o .

A. Specifications

The proposed single-stage TL-AS converter is designed to operate within an input line-to-neutral voltage variation of 170V to 265V, while providing 3kW at 48V to the output, and switching the power stage at 50kHz.

B. Duty Cycle

According to the characteristics of the single-stage TL-AS converter shown in Fig. 4-18, for a given normalized output power the intermediate bus voltage increases as the duty cycle increases. From this standpoint, the duty cycle cannot be too high. On the other hand, choosing a small duty cycle increases the current stresses in both the AC and DC sides. As a result of this trade off, the duty cycle for the design of the single-stage TL-AS converter has been chosen to be 0.25. This duty cycle is chosen to provide output voltage regulation at full load and low-line input voltage.

To optimize the design of the proposed single-stage TL-AS converter, the AC side must operate near the DCM/CCM boundary condition. The voltage gain at the DCM/CCM boundary is given by (4-18). Using the chosen duty cycle ($D=0.25$), the critical voltage gain at the DCM/CCM boundary is 2.67, which results in an intermediate bus voltage of 641V at low-line input voltage (170V).

C. Transformer Turns Ratio

Equation (4-21) can be rewritten as follows:

$$(4-27) \quad \frac{n_t V_o}{V_{bus}} = 2D(1-D) - \frac{4I_o L_r f_s}{n_t V_{bus}}.$$

The second term in (4-27) represents the duty-cycle loss in the DC side caused by the circulation of energy through the resonant inductor L_r . Increasing this term means increasing the load range in which the proposed converter operates with ZVS. On the other hand, increasing the duty-cycle loss also increases the circulating energy in the converter. Therefore, a duty-cycle loss of 20% with respect to the first term in (4-27) represents a good trade off between the ZVS range and the circulating energy in the converter.

The transformer turns ratio can then be calculated from (4-27) using the converter specifications at full load and low-line input voltage. At this operating point, the bus voltage is 641V, as discussed above, which yields a transformer turns ratio of $n_t=4$.

D. Resonant and Output Filter Inductance

The resonant inductance is obtained from the duty-cycle loss term, defined as follows:

$$(4-28) \quad D_{loss} = \frac{4I_o L_r f_s}{n_t V_{bus}}.$$

The calculation is performed at full load to guarantee regulation of the output voltage. Substituting all the pertinent values into (4-28) results in the resonant inductance $L_r=15.41\mu\text{H}$.

The trade offs in determining the output inductance are similar to those discussed for the single-stage TL-PS converter presented in the beginning of this chapter. Increasing the output inductance also increases the maximum intermediate bus voltage of the proposed single-stage TL-AS converter. An inductance ratio of $n_t^2 L_o/L_r = 8$ has also been used in the design of the proposed single-stage TL-AS converter, which results in an output inductance $L_o=7.68\mu\text{H}$.

E. Boost Inductance

The power delivered to the output is limited by the input boost inductances. According to (4-15), the normalized power delivered to the output at low-line input voltage and full load is $P_{on}=0.142$. The boost inductance can be obtained by de-normalizing (4-17), which results in $55\mu\text{H}$.

The use of AC capacitors to provide the artificial neutral point connection changes the AC input to the intermediate bus voltage converter gain. For this reason, when the boost inductance determined above is connected in the presence of the AC capacitors, it is observed that the boost inductor operates in a deeper DCM condition as compared to the theoretical prediction. Taking into account the design point at low-line input voltage and full load, the boost inductance has to be adjusted to $72\mu\text{H}$ in order to make the proposed converter operate as predicted in the design. The boost inductance at different switching frequencies can be determined from Fig. 4-20.

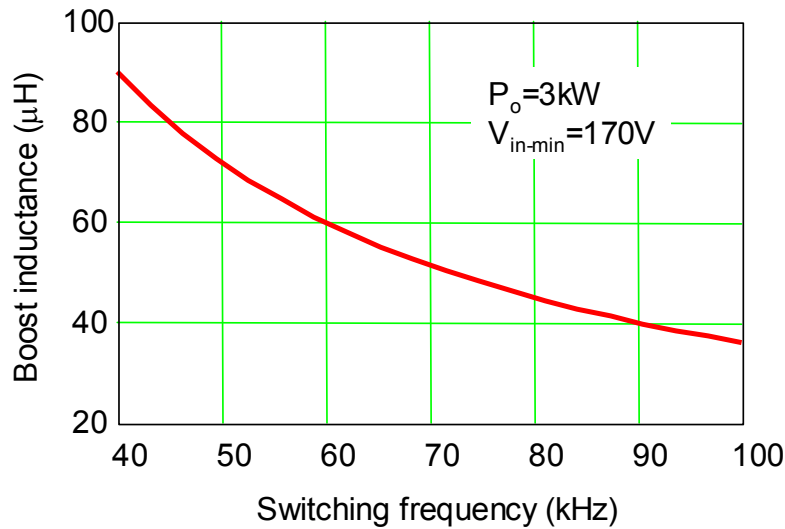


Fig. 4-20. Boost inductance as a function of the switching frequency for DCM operation.

4.4.4. Experimental Results and Comparisons

This section presents experimental results obtained from the single-stage TL-AS converter, and provides a comparison with the single-stage TL-PS converter discussed at the beginning of this chapter. Table 4-1 summarizes the various components used in the implementation of both converters. As can be seen, the major difference between them is that the transformer of the single-stage TL-AS converter requires more turns to account for the DC magnetizing current that results from the asymmetrical operation. The transformer core size, however, was the same for both single-stage converters.

Fig. 4-21(a) and Fig. 4-21(b) show the drain voltages and gate signals for switches S_1 and S_2 , respectively. As can be observed, both switches operate under ZVS, since the drain-to-source voltages reach zero before the gate signals are applied. These results have been obtained at 3kW of output power and 180V of line-to-neutral input voltage. Since the total intermediate bus

voltage at this operating point was 626V, one can see that the voltage stress across the switches is half of the total bus voltage.

Table 4-1. Components used in the implementation.

Component	Single-Stage Three-Level Phase-Shift Converter	Single-Stage Three-Level Asymmetrical Converter
Boost Inductance	110 μ H	72 μ H
Resonant Inductance	11 μ H	15 μ H
Output Inductance	5.7 μ H	7.7 μ H
Number of Turns	12/4/4	20/5/5
Blocking Capacitor	-	5u/1000V
Input Rectifiers	RUR30120	RUR30120
Output Rectifiers	HFA 120MD40D	HFA 120MD40D
Power Switches	IXFN 44N80	IXFN 44N80
Clamping Diodes	RUR30120	-

Fig. 4-21(c) shows the transformer primary current at full load and for three different input voltages. The asymmetrical characteristic of the converter can be seen in the figure, while the average current through the primary side of the transformer is zero. Fig. 4-21(d) illustrates the input current in one of the phases after the switching ripple has been filtered for three different input phase voltages. As observed, the harmonic distortion of the input current is dependent upon the input voltage.

Fig. 4-22(a) shows the intermediate bus voltage measured from the TL-AS converter for three different input phase voltages. The intermediate bus voltage increases as the output power decreases. In the same way as described before for the TL-PS converter, the explanation for this behavior is based on the power balance and the operating mode of the output filter inductor. For instance, suppose that the output inductor is operated in CCM and that the voltage drop across the resonant inductor can be ignored. Under these assumptions, the DC output voltage is simply a function of the duty cycle and intermediate bus voltage. If the load decreases, the duty cycle must also decrease to store less energy in the DCM boost inductors. Since the DC output voltage

is fixed and is a function of the duty cycle and intermediate bus voltage, one can conclude that decreasing the duty cycle has to be compensated for by increasing the intermediate bus voltage in order to maintain the DC output voltage regulation. This mechanism explains why the intermediate bus voltage increases as the output power decreases. Fig. 4-22(a) also shows a region at light load in which the intermediate bus voltage no longer increases. In that region, the output inductor starts operating in DCM. As can be seen, the intermediate bus voltage of the TL-AS converter reaches the same level at light load as the intermediate bus voltage of the TL-PS converter shown in Fig. 4-12(a).

As illustrated in Fig. 4-22(b), there is voltage stress across the DC blocking capacitor. For this reason, it is required that either polypropylene or metallic film capacitors be used in order to withstand the voltage stress, as well as to withstand the primary RMS current, which is 15A at full load and low-line input voltage.

Fig. 4-22(c) illustrates the efficiency comparison between three converters: (1) the two-stage front-end converter studied in chapter 3, (2) the single-stage TL-PS converter presented at the beginning of this chapter, and (3) the single-stage TL-AS topology under discussion. As predicted, the single-stage TL-AS converter presents improved efficiency when compared against the single-stage TL-PS converter. The same figure also shows the trade off between performance and cost. The two-stage approach presents the best efficiency of all cases under comparison, but its cost is also the highest.

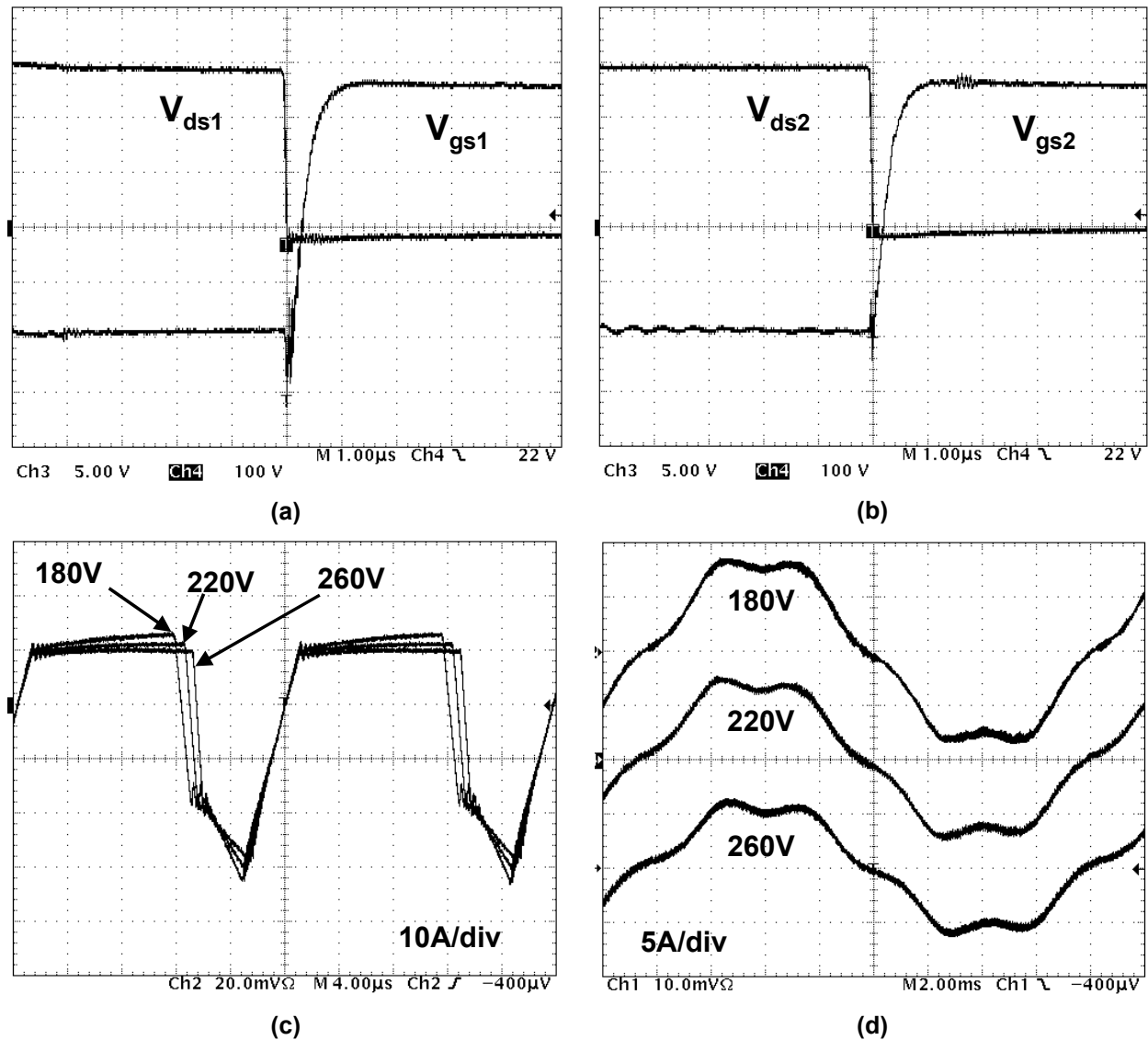


Fig. 4-21. Experimental results: (a) drain voltage and gate signal for S_1 at 3kW and $V_{in}=180V$, (b) drain voltage and gate signal for S_2 at 3kW and $V_{in}=180V$, (c) primary current at 3kW for three input voltages, and (d) filtered input current at 3kW for three input voltages.

The harmonic distortion comparison between the three cases is illustrated in Fig. 4-22(c). Despite presenting an efficiency improvement over the single-stage TL-PS converter, the TL-AS topology does not perform well in terms of THD. The lowest THD is obtained from the TL-PS converter, while the THD of the two-stage approach falls between the two single-stage converters.

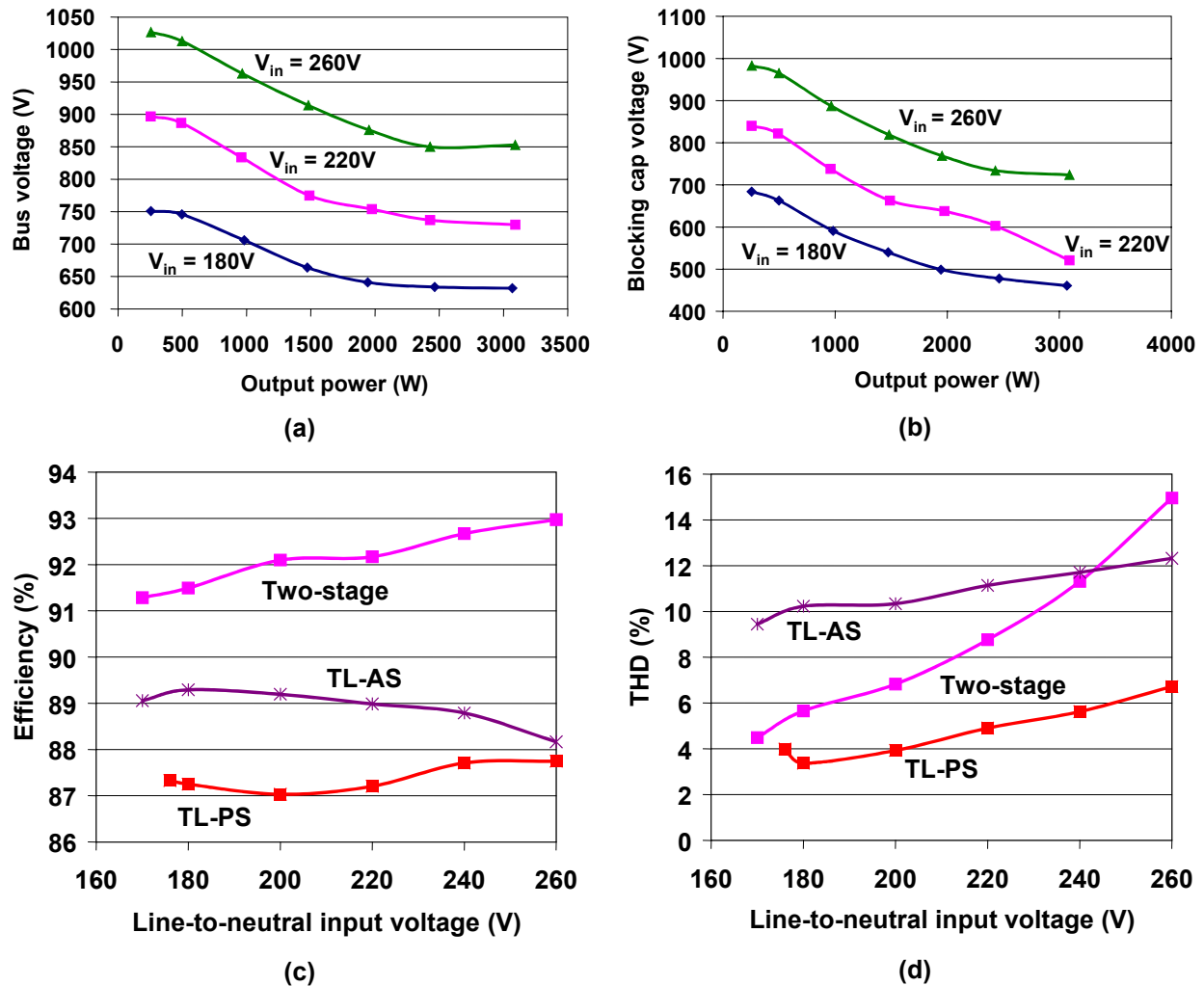


Fig. 4-22. Results and comparisons: (a) intermediate bus voltage stress, (b) DC blocking capacitor, (c) efficiency comparison, and (d) THD comparison.

4.5. Interleaved Single-Stage AC/DC Converters

Both single-stage three-level AC/DC converters operate under DCM. As a result, the input current ripple is significantly higher, as compared to boost-type CCM converters. This ends up increasing the size and volume of the EMI filter for DM noise. Interleaving can provide input current ripple cancellation to reduce these filtering requirements [83].

Fig. 4-23 shows both interleaved three-level single-stage converters used to provide input current ripple cancellation. The power stage is duplicated and the input filter is designed at the system

level. For two interleaved converters, the first high-frequency harmonic to be attenuated occurs at the side-band frequencies of $2f_s$, more specifically at $2f_s \pm f_r$, where f_s is the switching frequency and f_r is the line frequency.

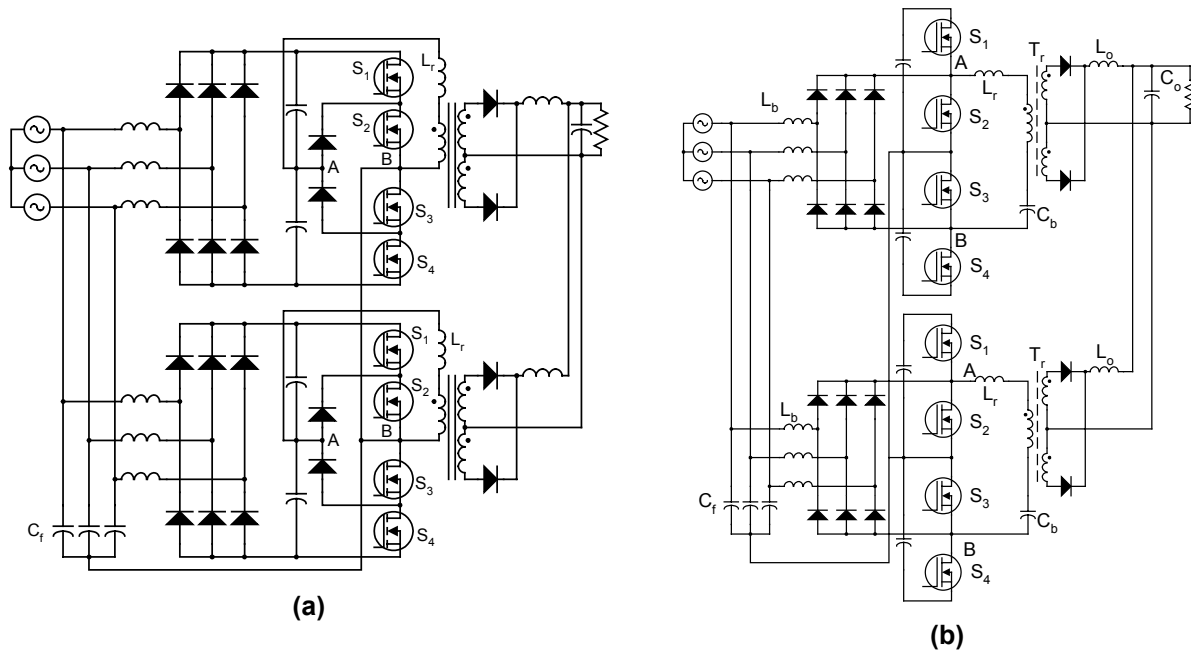


Fig. 4-23. Interleaved single-stage converters: (a) TL-PS and (b) TL-AS.

The amplitude of the relevant high-frequency harmonics to be attenuated is shown in Fig. 4-24 for both single-stage non-interleaved and interleaved systems. The total system power for both cases is 6kW, which results in 3kW per converter for the interleaved system and 6kW for the single converter used in the non-interleaved approach. As can be seen in Fig. 4-24, the odd harmonics are cancelled out in the interleaved systems, while the even harmonics present the same amplitude as those of the non-interleaved system. Another observation is that the interleaved single-stage TL-PS converter generates lower high-frequency harmonics than its counterpart single-stage TL-AS topology. Although the high-frequency harmonics have been provided for the non-interleaved converters, the following comparison will consider only the interleaved case.

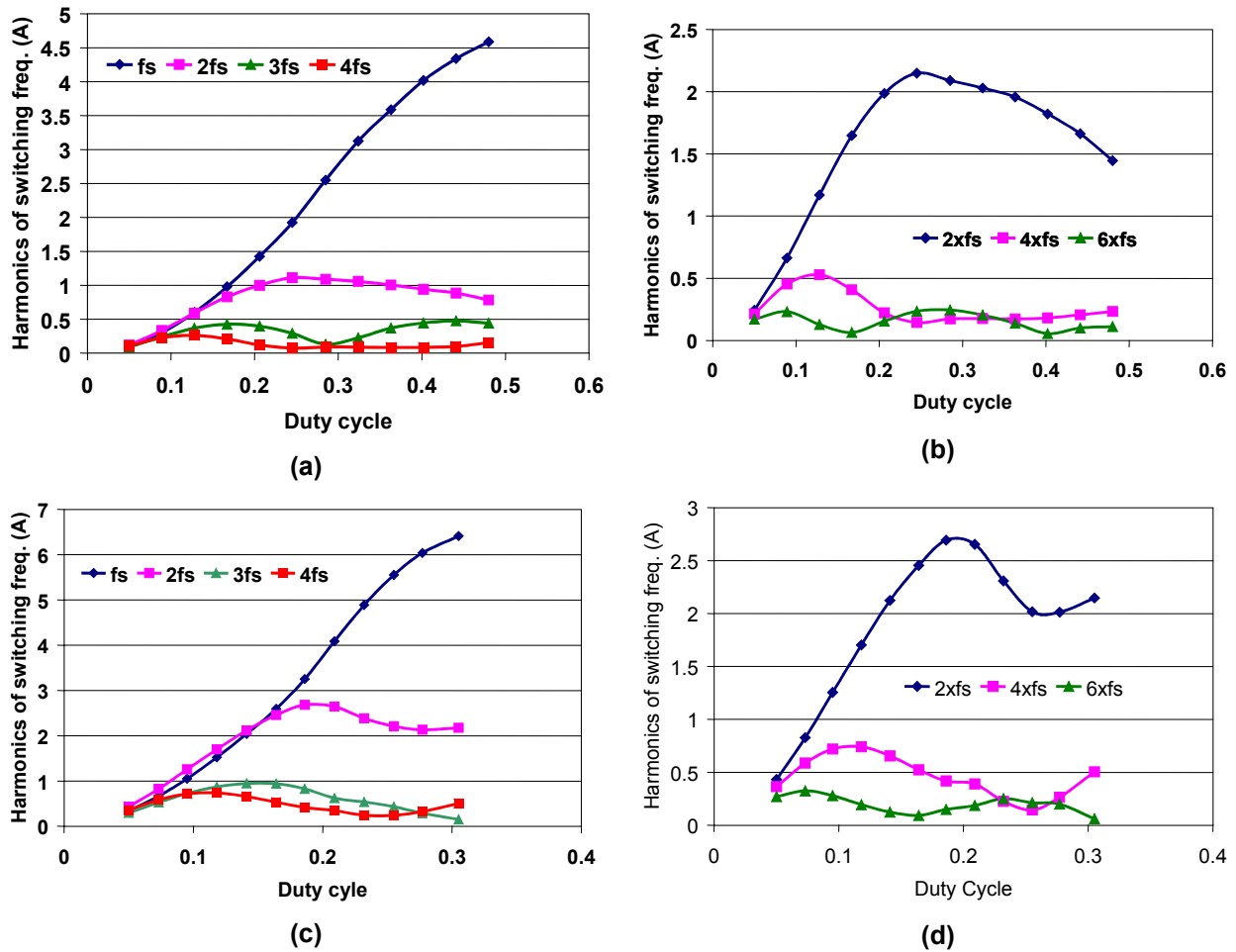


Fig. 4-24. Harmonics of switching frequency: (a) non-interleaved 6kW TL-PS, (b) interleaved 6kW TL-PS, (c) non-interleaved 6kW TL-AS, and (d) interleaved 6kW TL-AS.

Fig. 4-25 and Fig. 4-26 illustrate the calculation results for the size of boost and DM filter inductors using the CISPR 22 Class B as the conducted EMI standard. The calculation results obtained for the VDE standard will not be shown because the two previous chapters have demonstrated that interleaving is rather beneficial in reducing the DM filter size when the VDE standard is taken into account. The cases compared in the following two figures include: (1) the VIENNA rectifier (benchmark), (2) the two-switch interleaved rectifier, (3) the single-stage TL-PS converter, and (4) the single-stage TL-AS topology.

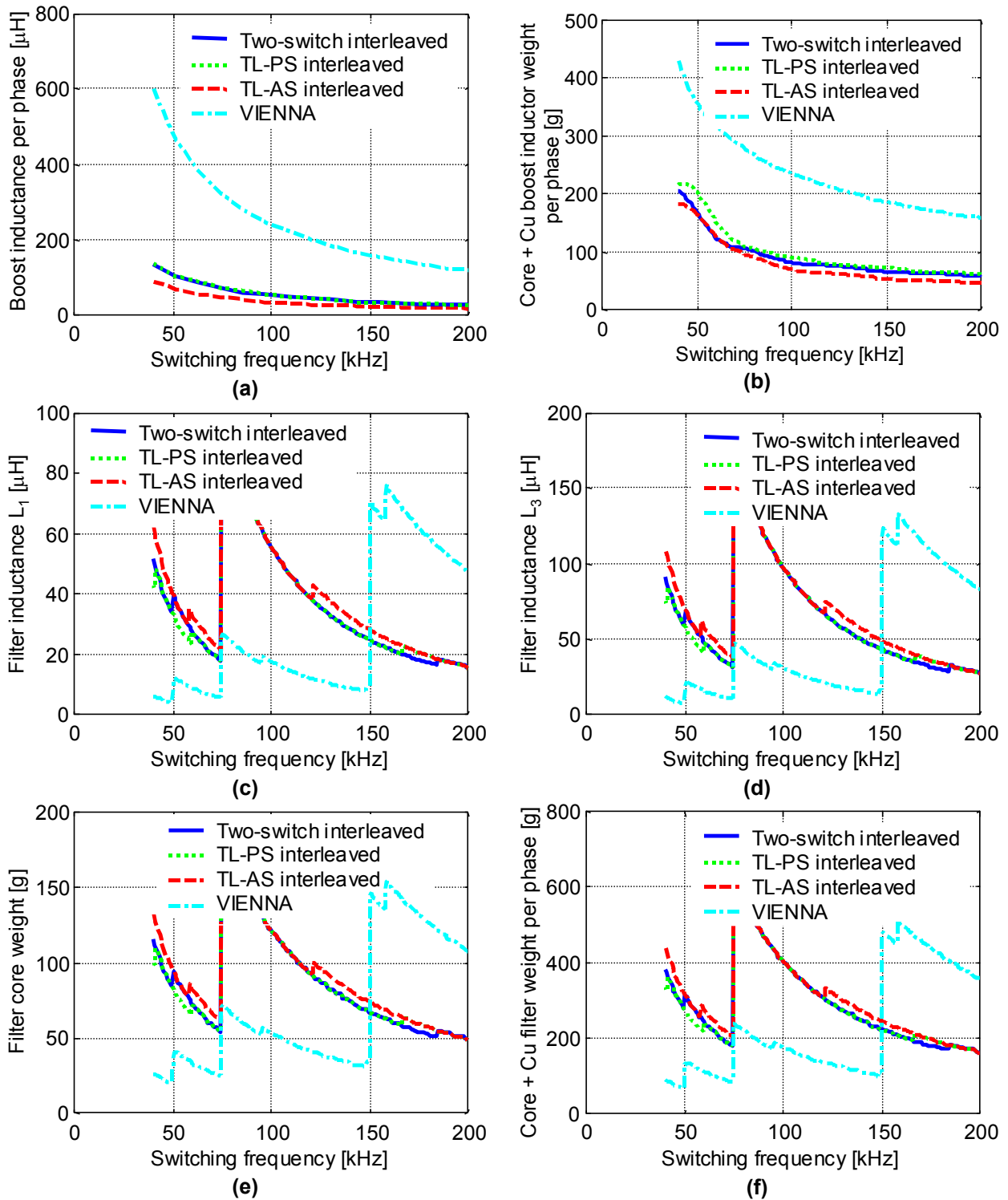


Fig. 4-25. Design results: (a) boost inductance, combined boost inductor core + Cu weight per phase, (c) filter inductance L_1 , (d) filter inductance L_3 , (e) filter core weight needed to implement $L_d+L_1+L_3$, and (f) Core + Cu weight per phase required to implement $L_d+L_1+L_3$.

Fig. 4-25(a) shows the boost inductance needed for each case, while Fig. 4-25(b) provides an estimation of the total weight of the boost inductors per phase. For the interleaved cases, Fig. 4-25(a) shows the value of each inductance, whereas Fig. 4-25(b) represents the weight of the two inductors connected to the same phase.

The amount of filter inductance needed per phase is shown in Fig. 4-25(c) and Fig. 4-25(d). All the interleaved systems require about the same amount of filter inductance per phase. Although the interleaved systems show advantages above 150kHz, the frequency range that is most suitable for the single-stage converters is from 40kHz to 70kHz, since the efficiency of the single-stage topologies is very low at high switching frequencies. For 40kHz to 70kHz, the VIENNA rectifier results in the least amount of filter inductance required to attenuate the DM noise. Fig. 4-25(e) and Fig. 4-25(f) confirm the fact that the filter required by the VIENNA rectifier is the smallest among the cases compared.

Although the VIENNA rectifier results in the smallest DM filter size, adding the size of the boost inductor to the size of the input filter in each phase changes the comparison. As shown in Fig. 4-26(a), the magnetic size for the combined boost and filter inductors in the switching frequency from 40kHz to 70kHz is decreased for the interleaved cases, while Fig. 4-26(b) includes the Cu weight in the comparison as well. According to Fig. 4-26(b), the region that most greatly reduces the boost and filter inductor size requirements is from 50kHz to 70kHz of switching frequency.

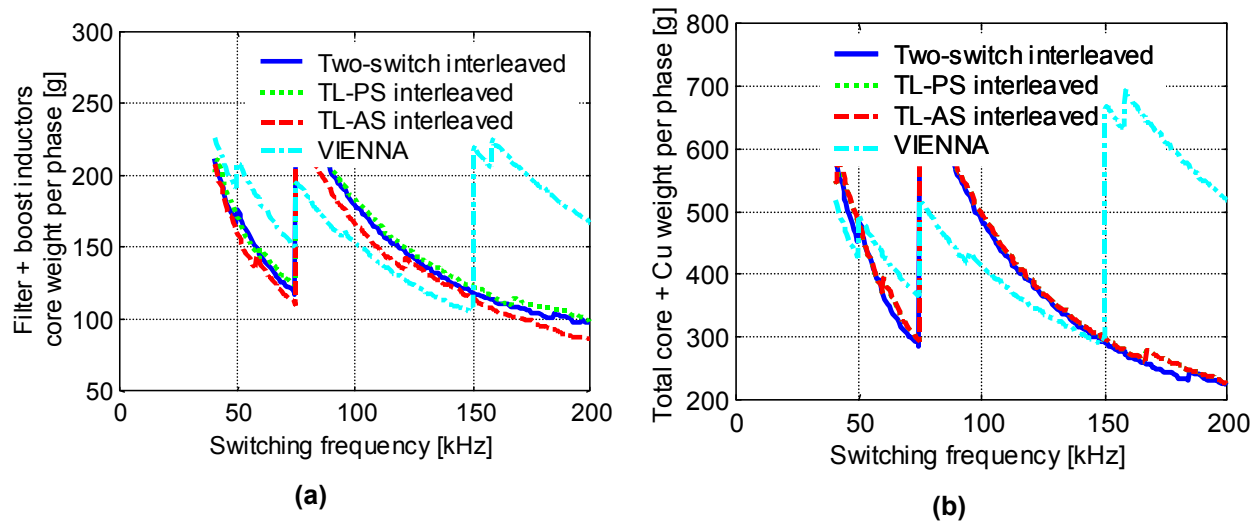


Fig. 4-26. Combined filter and boost inductor core weight per phase and (b) total core + Cu weight needed to implement the boost and filter inductors per phase.

4.6. Output Current Ripple Cancellation in Single-Stage Converters

The conditions at which interleaving the single-stage converters helps to cancel the DC output current ripple must still be determined. Cancellation of the output current ripple is beneficial to reducing the amount of output filter capacitance required to limit the output voltage ripple to below a specified limit.

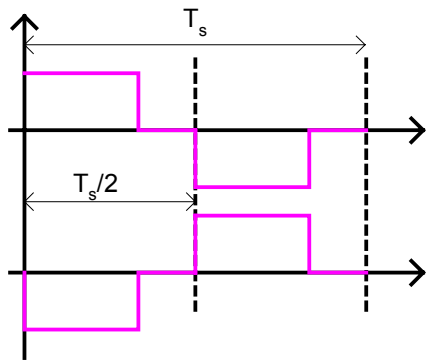
Fig. 4-27 and Fig. 4-28 illustrate how the output current ripple is canceled out when single-stage converters are interleaved. Fig. 4-27(a) shows both waveforms applied across points A and B when two TL-PS converters are interleaved (the points A and B are shown in Fig. 4-23(a)). As can be seen, the voltages across points A and B are symmetrical and phase shifted by 180° . Because of the symmetry of the waveforms, the rectified voltages applied across the input of the DC output filter are in phase with respect to each other. Therefore, the output filter inductor current ripples will not be interleaved. In fact, the output current ripple cancellation in interleaved single-stage TL-PS converters can only be achieved if more than two converters are interleaved at the same time.

Fig. 4-28 shows the theoretical waveforms related to the output current ripple cancellation in interleaved single-stage TL-AS converters. The voltages applied across points A and B are shown in Fig. 4-28(a) (the points A and B are shown in Fig. 4-23(b)). It can be seen from Fig. 4-28(a) that the primary voltages applied across points A and B are phase-shifted by 180° . These voltages are rectified and the waveforms applied across the output inductors are shown in Fig. 4-28(b). Differently from the interleaved TL-PS converters, the rectified waveforms in the TL-AS topologies are also 180° apart, which is a necessary condition to guarantee a phase-shift between the rectified voltage waveforms, as shown in Fig. 4-28(b). Therefore, the output inductor current ripples will be phase-shifted and interleaved to provide output current ripple cancellation, as illustrated in Fig. 4-28(c).

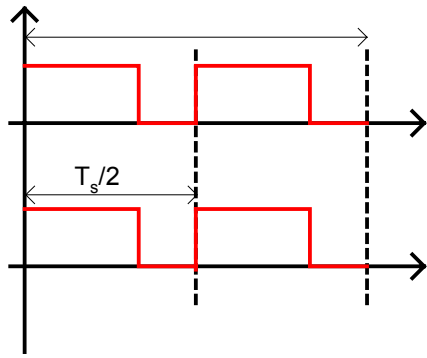
In summary, the TL-PS AC/DC converter will cancel out the output current ripple if and only if more than two converters are interleaved together. On the other hand, the single-stage TL-AS topology can provide output current ripple cancellation for any number of interleaved converters.

4.7. C-Message and Psophometric Noise Levels in Single-Stage Front-End Converters

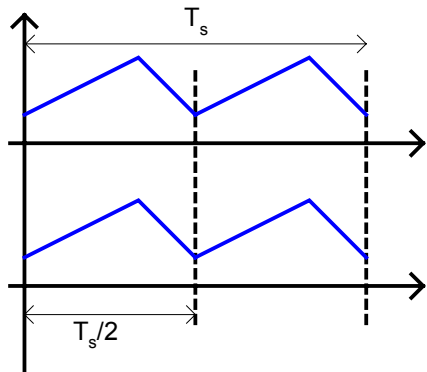
For telecom applications, it is important to limit the output noise voltage of front-end converters to avoid disturbance pickup in voice channels. Power supply manufacturers usually specify weighted C-message and psophometric noise for DPS telecom applications. There are several factors that affect the noise performance of rectifiers, such as the voltage regulation bandwidth and the impedances of installation and battery string.



(a)

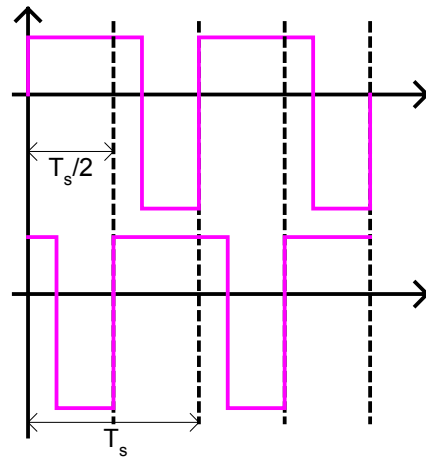


(b)

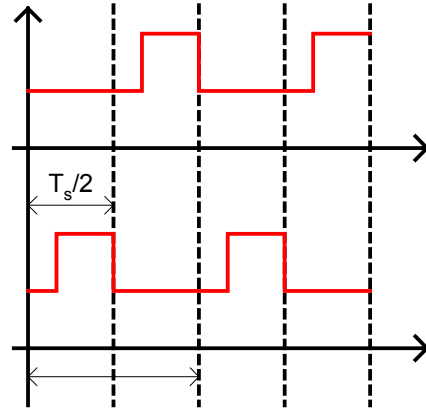


(c)

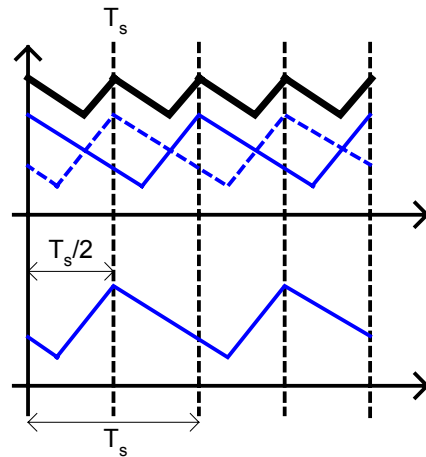
Fig. 4-27. Output current ripple cancellation in interleaved TL-PS converters: (a) voltage v_{ab} , rectified secondary voltage, and (c) output inductor currents.



(a)



(b)



(c)

Fig. 4-28. Output current ripple cancellation in interleaved TL-AS converters: (a) voltage v_{ab} , rectified secondary voltage, and (c) interleaved output inductor currents.

The ability of the front-end converter to fast regulate the output voltage is an important feature that helps to limit the noise amplitude in the frequency range of interest. In a two-stage approach, the fast output voltage regulation of the DC/DC converter guarantees that the noise generated in the frequency range of interest (100Hz to 5kHz) is filtered out in order to limit the C-message noise in the output voltage. It remains to evaluate if single-stage front-end converters can perform well in limiting C-message and psophometric noise levels.

Besides the influence of the front-end converter on the noise level, battery and installation impedances also affect the noise performance. The noise provided by power supply manufactures is measured under controlled laboratory conditions. However, if the same front-end converter is placed in a different installation, the noise level produced will vary according to installation and battery string impedances [84].

The objective of the following sub-sections is to demonstrate the ability of the single-stage front-end converters to constrain noise levels. The analysis is performed via Saber simulation, and several assumptions are used to approach the problem.

4.7.1. Voltage Loop Bandwidth of Single-Stage Front-End Converters

The magnitude of the C-message weighted noise can be determined according to the following relationship:

$$(4-29) \quad dBnrC = 20 \log \left(\frac{\sqrt{\sum_n (E_n w_n)^2}}{24.510^{-6}} \right),$$

where E_n is the RMS value of the noise voltage component, w_n is the weighing factor (C-message) at the component frequency f_n of interest, and $24.5\mu\text{V}$ is the reference noise voltage that results in 1pW of power in 600Ω reference impedance [84] [85]. Therefore, the contributing factors to the noise are the voltage level of the frequency components and the weighting factor at these frequencies. The C-message weighing factor is an experimentally determined relationship between the noise frequency and its disturbance effect on human hearing [84], as illustrated in Fig. 4-29.

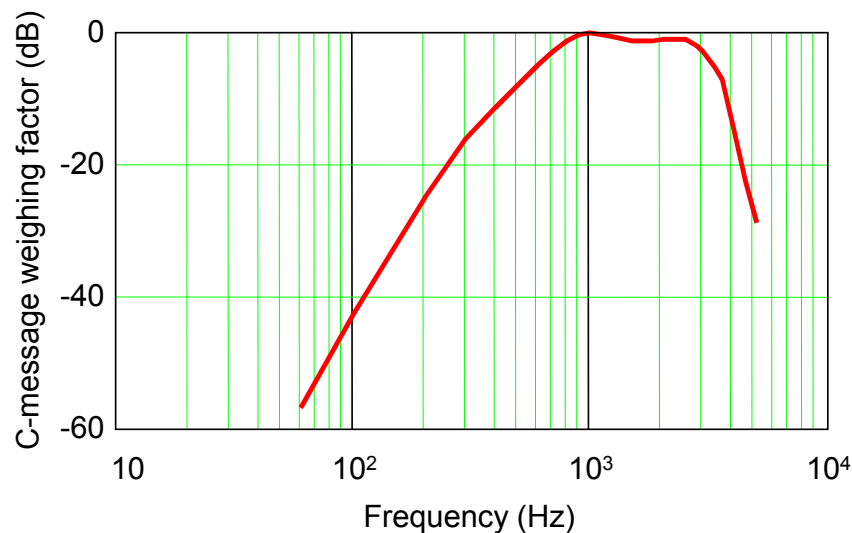


Fig. 4-29. C-message weighing factor.

As can be expected, the voltage control bandwidth of single-stage front-end converters plays an important role in limiting the C-message output voltage noise. Increasing the voltage control bandwidth certainly helps limit the output noise. In a two-stage approach, the voltage loop bandwidth of the DC/DC converter can be increased as much as possible to tightly regulate the output voltage, eliminating the problem of the C-message noise in the output voltage. However, it is unclear at this point if single-stage front-end converters can be implemented with a wide voltage control bandwidth without deteriorating the THD of the input currents. In fact, to answer

this question, the following paragraphs demonstrate that increasing the bandwidth of the voltage control does not deteriorate the THD of the input currents.

The single-stage TL-PS converter is taken into account in the following analysis. The small-signal modeling is an important step in order to design the voltage loop control bandwidth. Because the intermediate bus capacitor is large enough to store energy, it is assumed that both AC- and DC-side can be dynamically decoupled for small-signal perturbations. As a result, an equivalent three-level ZVS DC/DC converter can be used to represent the DC-side of the single-stage TL-PS converter. Moreover, this equivalent three-level DC/DC converter can be used to design the voltage loop of the single-stage topology. Three-level and full-bridge converters are identical from the small-signal standpoint, and for this reason the models developed for the phase-shifted full-bridge converters [86] can be readily applied to three-level phase-shifted ZVS DC/DC converters, as shown in Fig. 4-30.

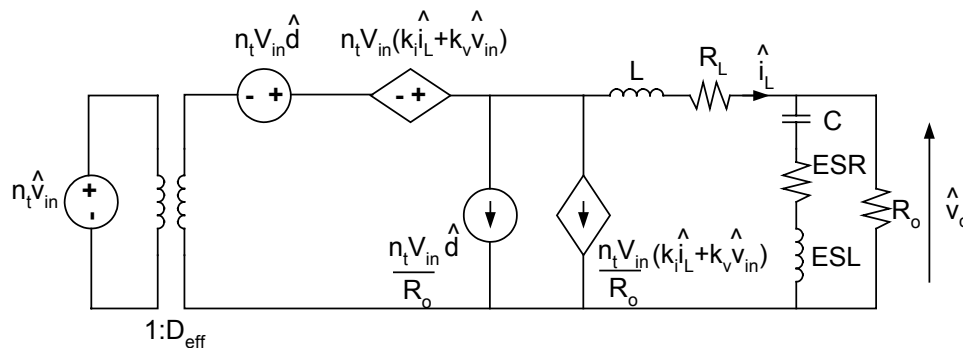


Fig. 4-30. Small-signal model of the equivalent three-level ZVS phase-shift DC/DC converter representing the DC section of the single-stage TL-PS converter.

To simplify the approach, the results analyzed hereafter have been obtained at a specific operating point for the single-stage TL-PS converter, which is 220V of input phase voltage, 3kW of output power, and 50kHz of switching frequency. At this operating point, the simulated bus voltage is 700V, which slightly differs from the experimental results shown in Fig. 4-12 because

the loss modeling has not been considered in this analysis. The various constants illustrated in Fig. 4-30 can be determined as follows:

$$\begin{aligned}
 k_i &= -\frac{R_d}{n_t V_{in}} \\
 (4-30) \quad k_v &= \left(I_L - \frac{V_o}{L} (1-D) \frac{1}{4f_s} \right) \frac{4n_t L_{lk} f_s}{V_{in}^2} v_{in} , \\
 R_d &= 4n_t^2 L_{lk} f_s
 \end{aligned}$$

where $V_{in}=351\text{V}$ (half of intermediate bus voltage), $n_t=4$, $I_L=62.5\text{A}$, $V_o=48\text{V}$, $L=5.7\mu\text{H}$, $D=0.34$, $L_{lk}=11\mu\text{H}$ and $f_s=50\text{kHz}$. The measured series resistance of the output filter inductor was $38\text{m}\Omega$. In order to limit the high frequency output ripple (not the C-message noise) to lower than 480mV , the equivalent series resistance of output filter capacitor has to be lower than $15\text{m}\Omega$. To accomplish this low ESR, seven capacitors of the type 380XL272M063J022 (Cornell Dubilier) were connected in parallel. The lead inductance per capacitor is estimated in 30nH , which results an equivalent lead inductance of 4.3nH .

The transfer function of interest is the duty ratio to the output voltage, which can be determined from the small-signal model shown in Fig. 4-30. The expressions obtained from that model are summarized as follows:

$$\begin{aligned}
 (4-31) \quad \hat{v}_o &= \frac{R_o \parallel \left(ESR + s ESL + \frac{1}{sC} \right)}{sL + R_L + R_o \parallel \left(ESR + s ESL + \frac{1}{sC} \right)} \left(n_t V_{in} \hat{d} + n_t V_{in} k_i \hat{i}_L \right) \\
 \frac{\hat{v}_o}{R_o} &= \frac{ESR + s ESL + \frac{1}{sC}}{ESR + s ESL + \frac{1}{sC} + R_o} \hat{i}_L
 \end{aligned}$$

From the previous expressions, the duty cycle to output voltage transfer function can be easily determined and the voltage loop control designed for a specified crossover frequency. As mentioned above, the objective is to verify the effect of the voltage loop control bandwidth on the THD of the input current, as depicted in Fig. 4-31. Increasing the control bandwidth has very little effect on the THD of the input current. This result represents an important outcome, since a wide control bandwidth is extremely desirable to reduce the C-message noise in the output voltage of single-stage front-end converters.

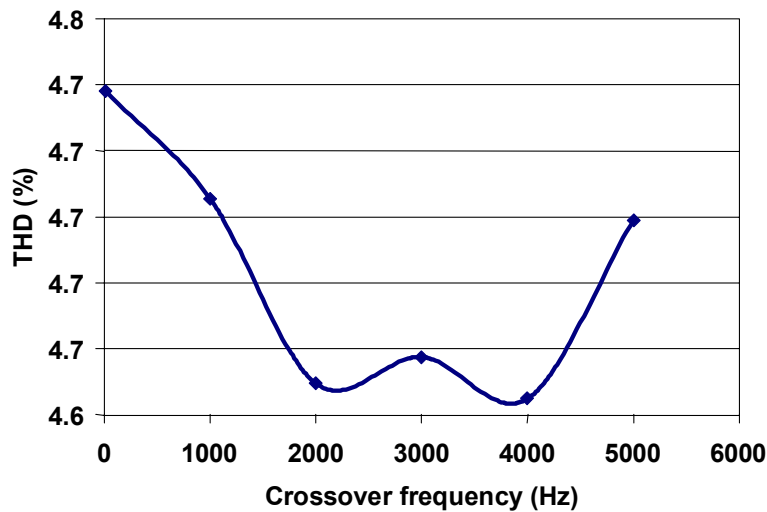


Fig. 4-31. Simulated input current THD as a function of the crossover frequency of the single-stage TL-PS converter.

4.7.2. Installation and Battery String Impedances

As concluded from the previous section, the voltage loop control bandwidth does not affect the THD of the input currents. Therefore, it remains to evaluate what role the control bandwidth plays in constraining the C-message noise across the output voltage. To proceed with this analysis, one can assume that the single-stage TL-PS converter is used to charge a battery string and to feed the load according to the installation previously described [85], as illustrated in Fig.

4-32(a). As can be seen, the battery string consists of 24 cells (GNB MAT-475, rated 475A-h at the 8h discharge rate). Each cell is connected by intercell busbars, while cables connect the ends of both rows. Fig. 4-32(b) shows the equivalent circuit for each section of the installation.

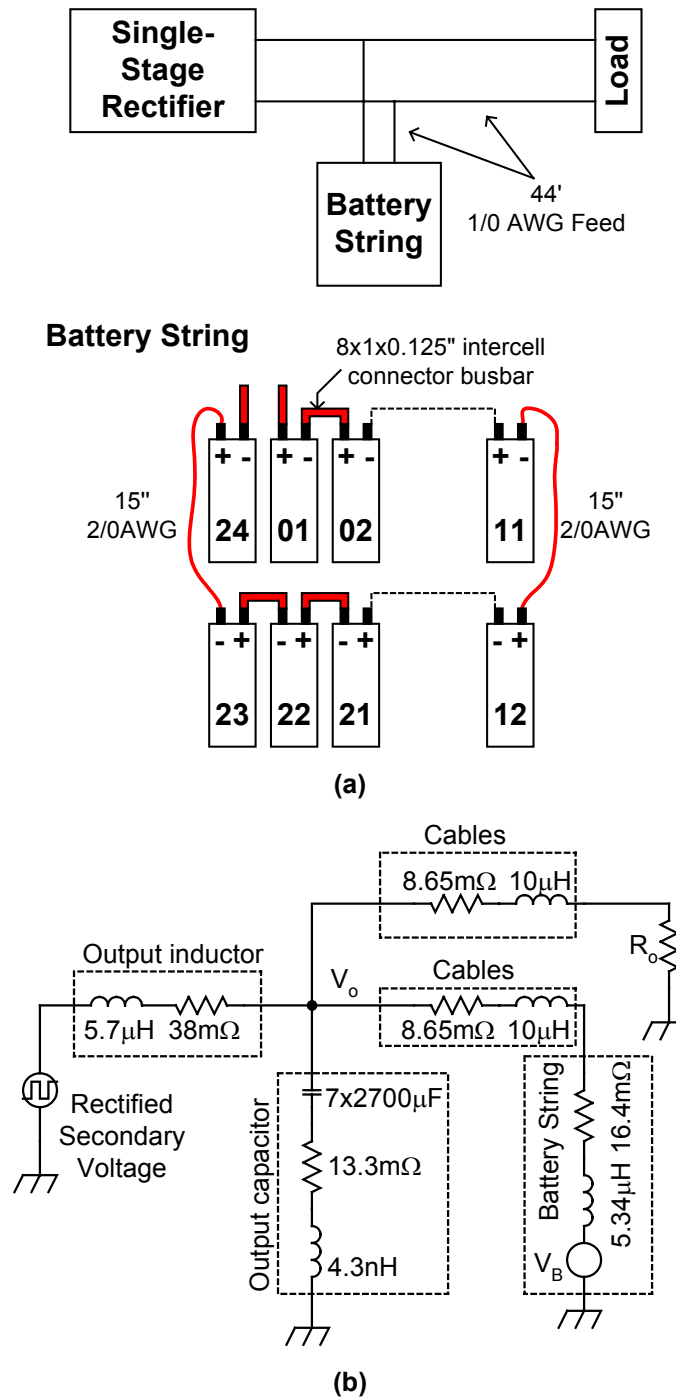


Fig. 4-32. (a) Installation and battery string configuration and (b) equivalent circuit.

Simulations using the single-stage TL-PS front-end converters have been performed to evaluate the noise in the output voltage. The intermediate bus capacitors of the single-stage TL-PS converter have been fixed to 100 μ F each for all simulations, while the DC output section has been implemented with the equivalent circuit shown in Fig. 4-32(b). The voltage loop control bandwidth has been adjusted according to the discussion in the previous section. The closed loop circuit has been simulated in Saber and the C-message noise determined according to (4-29) and the weighting factor illustrated in Fig. 4-29. The C-message noise in the output voltage is shown in Fig. 4-33(a), while the psophometric noise is shown in Fig. 4-33(b). The psophometric noise is determined using the conversion expression described below:

$$(4-32) \quad mV_{ps0} = 10^{\left(\frac{dBnrC-32.5}{20}\right)},$$

where mV_{ps0} is the psophometric noise in the output voltage given in mV and dBnrC is C-message noise given in dB.

As observed in Fig. 4-33, the noise in the output voltage decreases with the increase of the voltage loop control bandwidth. As mentioned earlier, power supply manufactures usually specify the psophometric noise below 2mV. Therefore, the single-stage TL-PS front-end converter can easily meet the specifications for psophometric noise in the output voltage.

4.8. Benchmarking

Since the single-stage front-end converters incorporate the DC power conversion function, the benchmark circuit for comparison shown in Table 4-2 includes a full bridge ZVS DC/DC converter. The data shown in Table 4-2 were obtained at 220V line-to-neutral input voltage. As

expected, the main drawbacks of the single-stage converters are the voltage stress across the power switches and the switch RMS current. The bus capacitance for hold-up time requirement in the single-stage front-end converters also increases because the intermediate bus voltage fluctuates according to load and input voltage variations, as opposed to the benchmark circuit that regulates the intermediate bus voltage to 800V. In terms of output filter capacitor, if one-stage output LC filter is used, then the single-stage front-end converters also require more capacitors to limit the high frequency output voltage ripple. More capacitors are required because the output inductor of the single-stage front-end converters operates closer to DCM in order to limit the intermediate bus voltage. As a result, the main motivation to develop single-stage front-end converters is cost reduction, which must be traded off for performance.

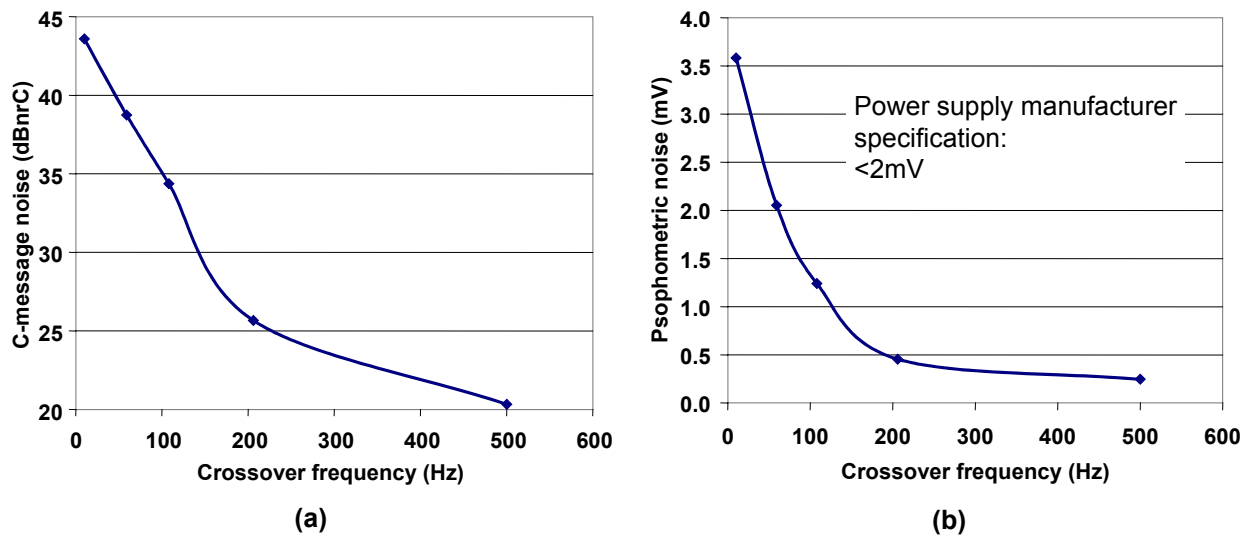
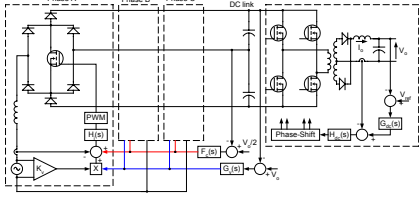
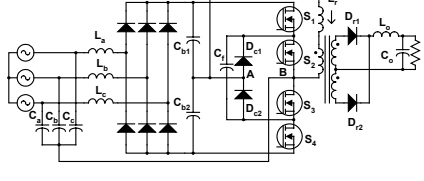
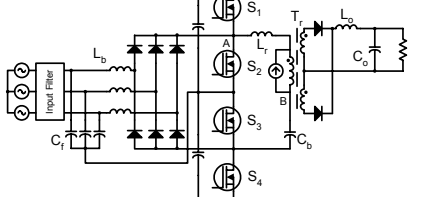


Fig. 4-33. (a) C-message output voltage noise and (b) psophometric noise.

Table 4-2. Benchmarking the single-stage front-end converters ($V_{in}=220V$ LN).

Topology Feature	VIENNA Rectifier and DC/DC converter 	Single-Stage Three-Level Phase-Shift (TL-PS) Converter 	Single-Stage Three-Level Asymmetrical (TL-AS) Converter 
Total power (kW)	3	3	3
Switches	7	4	4
Line freq. diodes	12	-	-
Fast diodes	8	10	8
Bus voltage (V)	800	1060	1060
Switch voltage (V)	400	530	530
RMS switch current (A)	2.8 (PFC circuit) 5.4 (DC/DC converter)	14.9 (outer switches) 20.3 (inner switches)	12.9 (outer switches) 16.8 (inner switches)
Intermediate cap RMS current (A)	5.6	10.9	12.9
THD (%)	-	4.7	11.2
Efficiency (%) at 50kHz	-	87	89
Power under two-phase operation (kW)	2	1.6	1.4
20ms holdup time intermediate bus cap (μF)	860 μF each cap	1430 μF each cap	1430 μF each cap
Output filter cap (μF)	3x2700 μF (380LX272M063J022 CDE)	7x2700 μF (380LX272M063J022 CDE)	8x2700 μF (380LX272M063J022 CDE)
Active current control	Yes	No	No
Sensing effort	High	Low	Low
Control complexity	High	Low	Low

4.9. Conclusion

This chapter presented two approaches for single-stage converters based on three-level topologies: (1) the single-stage TL-PS converter and (2) the single-stage TL-AS converter. The proposed converters provide zero-voltage turn-on and reduce the voltage stress applied across the power switches to 50% of the intermediate bus voltage. Syntheses of the switching power stages, along with analyses, designs, experimentation and comparisons have been provided for applications at 3kW and 48V DC output voltage.

The single-stage TL-PS converter was the first topology derived in this chapter to perform both PFC and DC output voltage regulation functions. The phase-shift modulation is implemented with commercial chips, such as those used for ZVS full-bridge converters. The THD of the input currents at full load is always lower than 7%, despite the simplicity of the circuit. The intermediate bus voltage becomes an issue in the design because the converter is able to regulate only the DC output voltage, while the voltage across the intermediate bus voltage fluctuates according to load and input voltage variations. It was found that a possible way to limit the increase of the intermediate bus voltage is to force the output filter inductor to operate in DCM. In this case, the maximum intermediate bus voltage decreases with the decrease of the output inductance. However, very low output inductance deteriorates the converter efficiency because the current stress increases in the primary switches. The switching frequency plays an important role in the overall efficiency of the AC/DC TL-PS converter. Because the input inductors operate in DCM, the turn-off instant of the power switches occurs when the input currents reach their peak value within the switching period. As a result, the switching losses are high, thus requiring

the switching frequency to be lowered to 50kHz in order to result in an overall efficiency greater than 87%.

The second single-stage converter proposed in this chapter was the TL-AS topology, which was proposed to improve the efficiency by reducing conduction loss. Indeed, the experimental results show an improvement in the overall efficiency as compared to the single-stage TL-PS converter. Despite improving the overall efficiency, the single-stage TL-AS topology presented a THD that was not as good as the THD presented by its TL-PS counterpart. The other drawback presented by the TL-AS topology is the voltage applied across the DC blocking capacitor, which requires the use of either polypropylene or film capacitors. The transformer also needs more turns in the primary side in order to compensate for the DC magnetizing current that builds up during the circuit operation. Despite these drawbacks, the TL-AS topology requires a minimal number of components, which is an advantage in reducing overall cost.

This chapter also explored the interleaving of single-stage AC/DC converters. It was demonstrated for CISPR 22 Class B standard that the size of DM filter inductors is still larger than the size required by the VIENNA rectifier (benchmark circuit). However, the interleaving of two single-stage converters helps reduce the overall combined sizes of filter and boost inductors, as compared to the VIENNA rectifier. The best practical switching frequency range for the design of interleaved single-stage AC/DC converters is between 50kHz and 70kHz. A great reduction in the overall size of boost and filter inductors occurs above 150kHz, but at this switching frequency range the design of single-stage converters is impractical due to the reduced efficiency.

In addition to canceling the input current ripple, one can also take advantage of the interleaving technique to provide cancellation for the OUTPUT current ripple. More than two interleaved converters are needed to provide output current ripple cancellation when single-stage TL-PS converters are used, while for the TL-AS topology any number of interleaved channels results in output current ripple cancellation.

In general, the performance of two-stage front-end converters is superior when compared to single-stage topologies. However, cost has been the driving force behind the developments described in this chapter. Despite the verified improved efficiency of the TL-AS approach, the single-stage TL-PS converter provides much lower THD, as well as lower stress to the transformer, which makes this circuit the best choice for single-stage front-end converters. In terms of C-message and psophometric noise levels, the TL-PS converter is able to constrain the noise when the voltage loop control bandwidth is properly designed. As a result, single-stage converters can also be used for telecom applications.

5. Simplified Interleaved Single-Stage AC/DC Front-End Converter

5.1. Introduction

As demonstrated in the previous chapters, the interleaving of DCM boost rectifiers is very effective in reducing the overall size of the boost and DM filter inductors when the CISPR 22 Class B standard is taken into account for determining the required filter attenuation. For the VDE 0871 Class B standard, the interleaving clearly reduces the size of the DM filter because the standard starts limiting the noise at 10kHz, as opposed to the CISPR 22 that limits the first high frequency noise at 150kHz. As a result, the reduction of the DM input filter size due to interleaving is not achieved for CISPR 22, but it is clear that interleaving helps reduce the requirements for magnetic components, since the overall size of boost and DM filter inductors is rather reduced when interleaving is used, as compared to VIENNA rectifiers.

Although the interleaving of DCM boost rectifiers has demonstrated advantages, all approaches that have been presented to this point require doubling the switching power stage. As a result, the number of components in the interleaved front-end converter is also doubled, which may incur a cost increase and additional layout space to accommodate the devices and interconnects for the interleaved system. To overcome this drawback, this chapter presents a simplified interleaved single-stage converter that eliminates the need for doubling the entire switching power stage in order to achieve input current ripple cancellation. Comparisons are also provided to illustrate the effectiveness of the novel interleaving technique. The analysis starts with a single-phase circuit,

and then the results are extended to three-phase applications. Experimental results taken from a 3kW prototype support the analysis.

5.2. Single-Phase Topology and Operating Principle

The circuit topology proposed in this chapter is illustrated in Fig. 5-1. As can be seen, the circuit is built on a three-level structure used to reduce the voltage stress applied across the power switches. The circuit is similar to its three-phase counterpart, the TL-PS converter presented in chapter 4, except for the addition of the auxiliary windings N_a that operate as magnetic switches. To provide proper operation for the magnetic switches [87], the number of turns of the auxiliary windings must be greater than $2N_p$. The conduction paths for the inductances L_1 and L_2 are required to be the same, otherwise the input current ripple cancellation will not be effective.

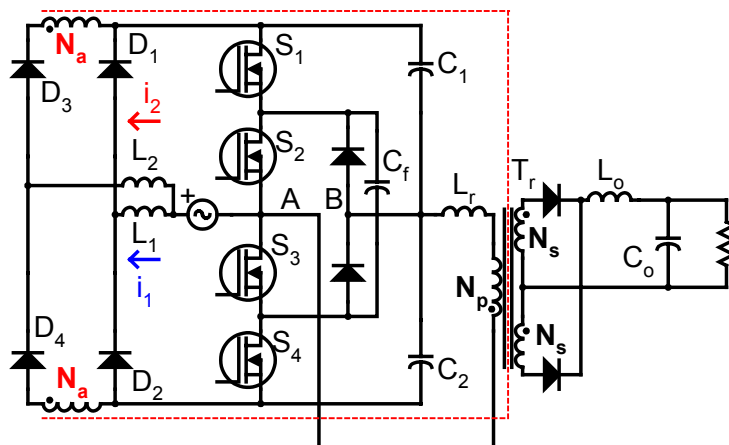


Fig. 5-1. Proposed interleaved single-stage/single-phase three-level phase-shift converter.

The following assumptions are taken into consideration for describing the operation of the circuit: (1) the input voltage is considered constant over a switching period, (2) the diodes and switches are ideal, and (3) the inductance L_r is ignored in the analysis (the impact of the transformer leakage inductance will be considered later on).

There are four main operating stages that are described in the following paragraphs, and the main waveforms are shown in Fig. 5-2. The switches are operated with 50% duty cycle, and phase-shift modulation is used to control the DC output voltage. No dead time can be seen between the gate signals shown in Fig. 5-2. Evidently, in practical applications, a small dead time is required to avoid shoot-through of the power switches.

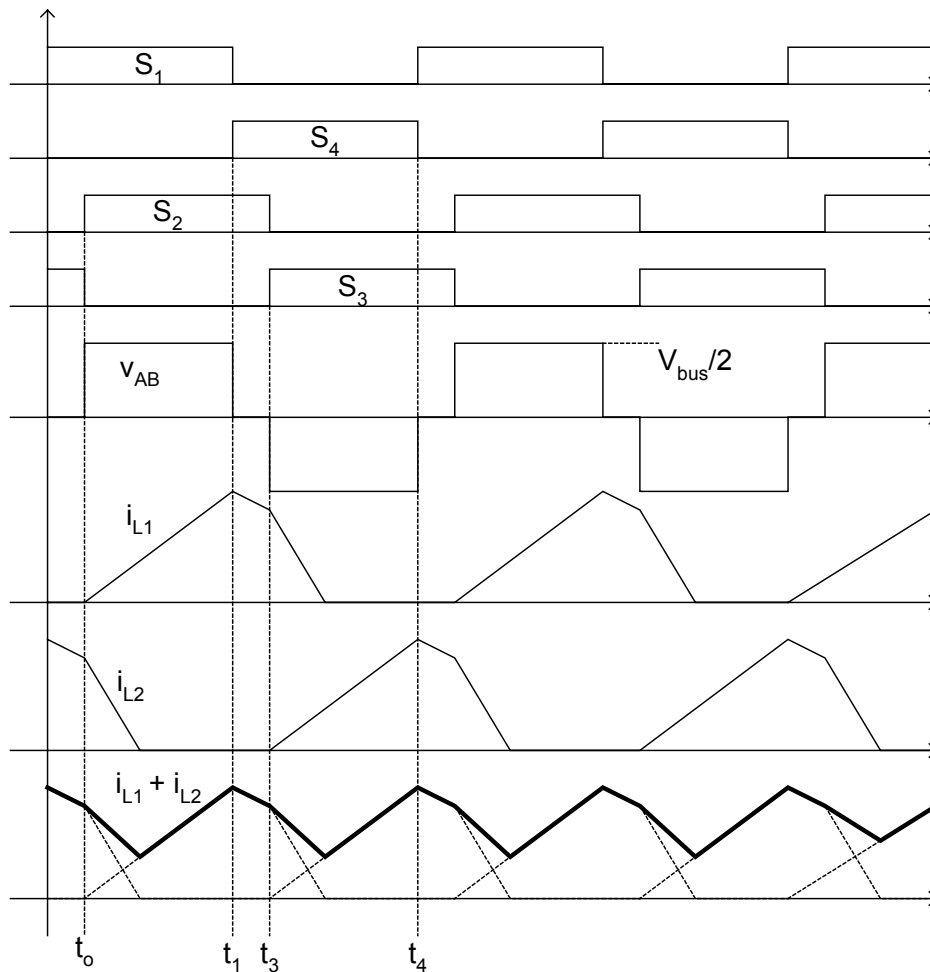


Fig. 5-2. Main waveforms.

Stage 1 (t_0, t_1) - Fig. 5-3(a): At instant t_0 , the switch S_2 is turned on and then power is transferred to the output. As a result, the current in inductor L_1 will increase linearly during this stage. Due to the polarity of the auxiliary windings, the current through inductor L_2 will be reset by the

voltage difference ($kV_{\text{bus}} - |v_{\text{in}}|$). The minimum bus voltage is designed to be greater than twice the peak input phase voltage. As a result, the current in inductor L_2 is fully reset during this stage.

Stage 2 (t_1, t_2) - Fig. 5-3(b): At instant t_2 , not shown in Fig. 5-2, the switch S_1 is turned off, and the energy stored in inductor L_1 is used to charge and discharge the intrinsic capacitances of S_1 and S_4 , respectively. This voltage transition is not shown in either Fig. 5-2 or Fig. 5-3, but when the discharge is complete, the body diode of S_4 will conduct to finalize the zero-voltage transition for S_1 and S_4 . The conduction of the body diode of S_4 slightly discharges the clamping capacitor C_f until the voltage applied across S_1 reaches the voltage across the bus capacitor C_1 , thus turning on the diode D_{c1} . Since the body diode of S_4 conducts during this stage, the switch S_4 can be turned on under ZVS. During this stage both currents through L_1 and L_o are partially reset. While the voltage difference ($V_{\text{bus}}/2 - |v_{\text{in}}|$) resets L_1 , the output voltage is used to reset L_o . The voltage across the auxiliary windings is zero because the voltage applied across points A and B is also zero.

Stage 3 (t_2, t_3) - Fig. 5-3(c): During this stage, the clamping diode D_{c1} conducts, while the currents through L_1 and L_o continue to be reset. The voltages across the auxiliary windings continue to be zero because v_{AB} is shorted out by the clamping diode D_{c1} . This stage is finished when switch S_2 turns off.

Stage 4 (t_3, t_4) - Fig. 5-3(d): When the switch S_2 is turned off, the boost inductor current flowing through L_1 will charge and discharge the intrinsic capacitances of S_2 and S_3 , respectively. When the voltage applied across S_3 reaches zero, the body diode of S_3 will conduct to finalize the ZVS turn on for S_3 . During this stage, the voltage polarity applied across points A and B is reversed, which enables the voltage applied across the auxiliary windings to be reversed as well. As a

result, this stage is characterized by the linear charge of the current in L_2 . During this stage, the inductor L_1 is fully reset by the voltage difference ($V_{bus}-|v_{in}|$). The fourth operating stage ends when the switch S_4 turns off. Then, the energy stored in L_2 will charge and discharge the intrinsic capacitances of C_4 and C_1 , respectively.

This operating stage can also be used to derive the turns ratio between the primary and auxiliary windings of the transformer. From the circuit shown in Fig. 5-3(d), the following expression can be obtained:

$$(5-1) \quad v_{L_2} = |V_{in}| + k V_{bus} - V_{bus} .$$

To guarantee that L_2 is magnetized at the same rate as L_1 , the constant k shown in (5-1) must be $k=1$.

From the circuit diagram, the voltage applied across the auxiliary winding is given by:

$$(5-2) \quad k V_{bus} = \frac{N_a}{N_p} \frac{V_{bus}}{2} .$$

Thus, in order to provide the same conduction path for both boost inductors L_1 and L_2 , the turns-ratio between the auxiliary and primary windings for $k=1$ must be:

$$(5-3) \quad \frac{N_a}{N_p} = 2 .$$

5.3. Extending the Principle to Three-Phase Applications

The proposed technique for simplifying the interleaving of the single-stage TL-PS converter is easily extended to three-phase applications. As shown in Fig. 5-4(a), the approach involves

adding two more legs to the circuit in order to obtain a three-phase converter. The same constraints described above for the single-phase converter, such as the transformer turns ratio between the primary and auxiliary windings, still apply for the three-phase circuit.

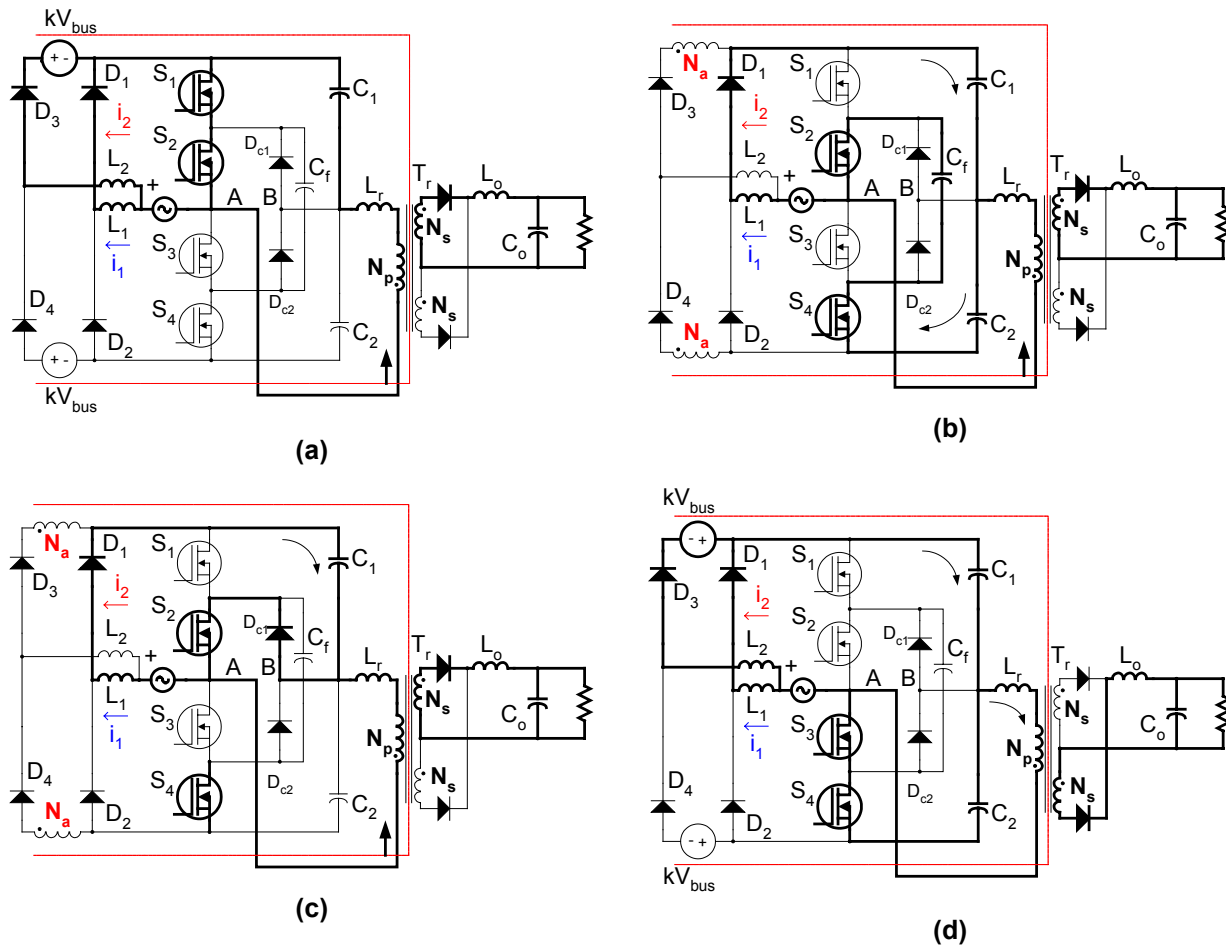


Fig. 5-3. Operating stages: (a) first stage (t_0, t_1), (b) first stage (t_1, t_2), (c) first stage (t_2, t_3), and (d) first stage (t_3, t_4).

In the three-phase simplified interleaved converter shown in Fig. 5-4(a), the neutral of the power system is connected to the switching power stage, which allows zero-sequence-order harmonics to circulate in the input lines. To eliminate this problem, the circuit shown in Fig. 5-4(b) employs three AC capacitors to generate an artificial neutral connection point in order to trap zero-sequence-order harmonics inside the converter.

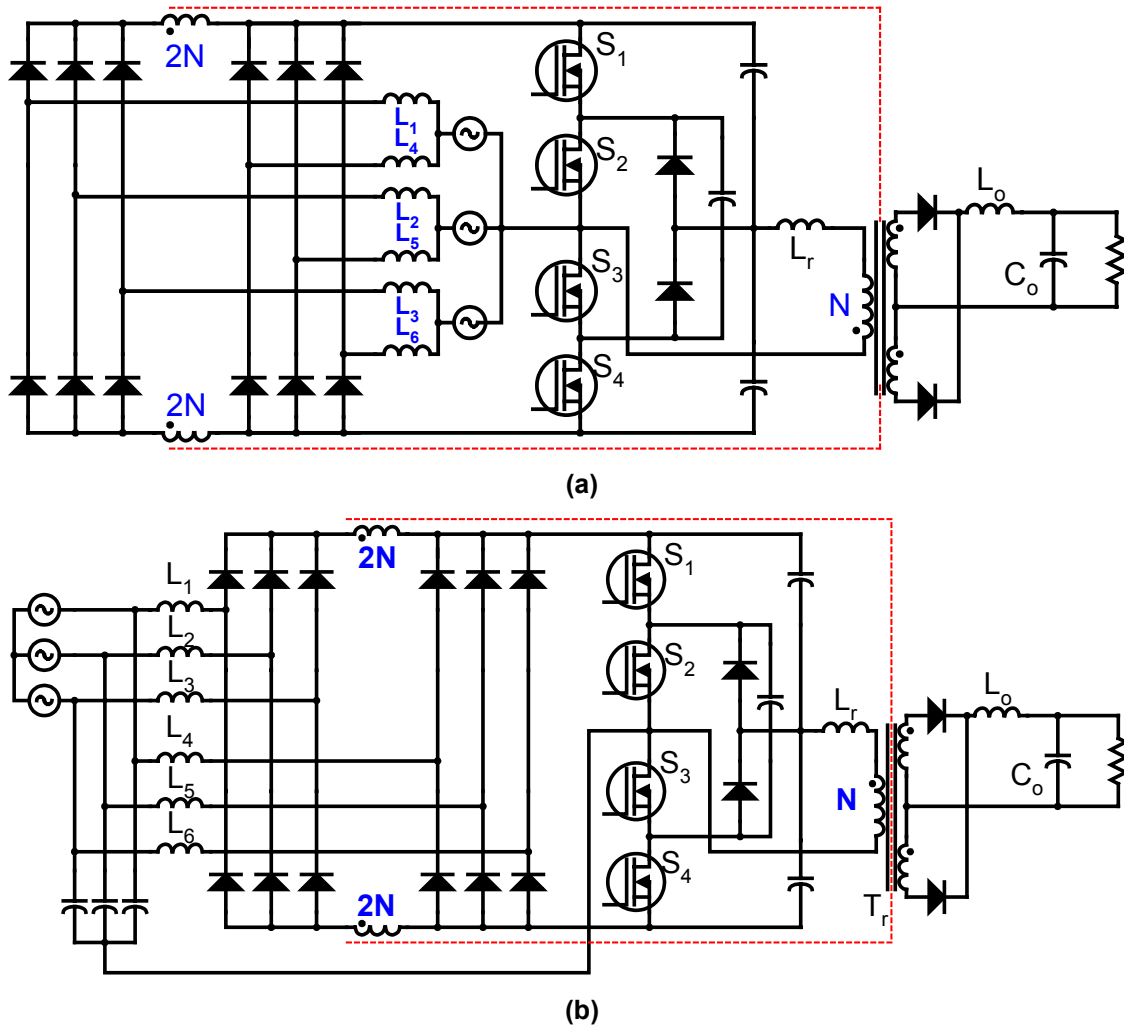


Fig. 5-4. Simplified three-phase interleaved converter: (a) simplified interleaved single-stage TL-PS converter, and (b) including AC capacitors to eliminate the neutral point connection of the power system.

5.3.1. Impact of the Resonant Inductance on the Effectiveness of Input Current Ripple Cancellation

The resonant inductance L_r results from the series combination of the transformer leakage inductance and any external inductance added to extend the ZVS operation of the proposed converter. The effect of the resonant inductance is to produce a voltage drop across the primary

side of the transformer, which is reflected to the auxiliary windings. As a result, the input current ripple cancellation is affected by the resonant inductance as well.

To evaluate the effect of the resonant inductance on the input current ripple cancellation, suppose that the proposed simplified interleaved converter has been designed to deliver 3kW of output power at a switching frequency of 50kHz. In this case, the boost inductances are 220 μ H, the output filter inductance is 5.7 μ H, the transformer turns ratio from the primary to the secondary is 4:1 (main turns ratio), and the transformer turns ratio from the auxiliary windings to the primary is 2:1 (auxiliary turns ratio).

Fig. 5-5 and Fig. 5-6 show the simulation results obtained from the proposed circuit illustrated in Fig. 5-4(b) using the design parameters described above. In the first simulation, the resonant inductance was set to 2 μ H, while in the second case it was set to 5 μ H. The first observation that can be made is that the current in inductor L_4 is always lower than the current in inductor L_1 because the voltage drop across the resonant inductor reduces the voltage reflected across the auxiliary windings. The impact of the voltage drop across the resonant inductance on the waveform of the interleaved current can be seen in Fig. 5-5(c) and Fig. 5-6(c), which show that the input current ripple cancellation effectiveness decreases as the resonant inductance increases. As a result, the noise at the switching frequency is not fully cancelled out because of the voltage drop across the resonant inductance. As illustrated in Fig. 5-6(d), the noise at the switching frequency becomes comparable to the noise at $2xf_s$, which was supposed to be the dominant high-frequency harmonic for two interleaved boost inductor currents.

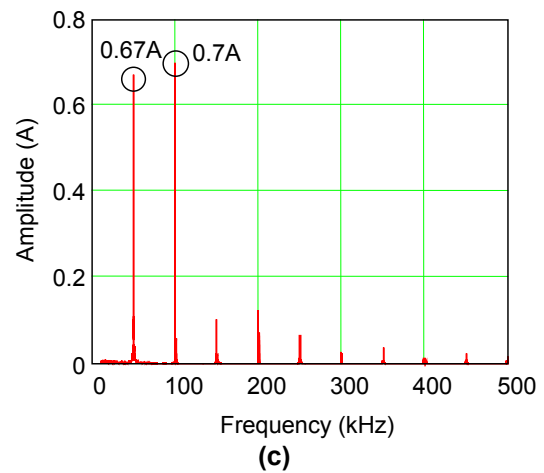
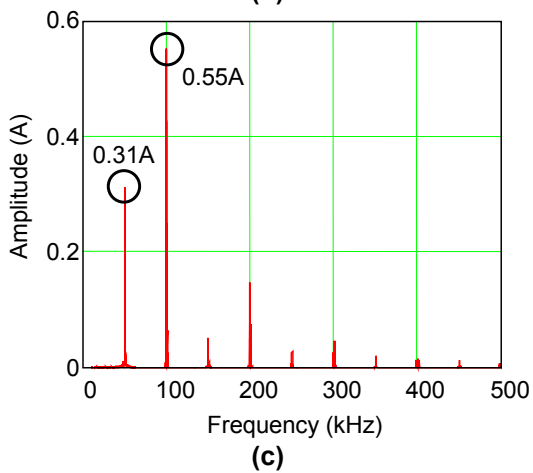
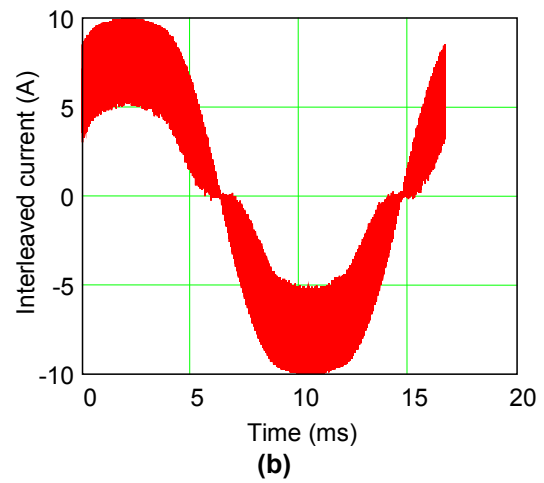
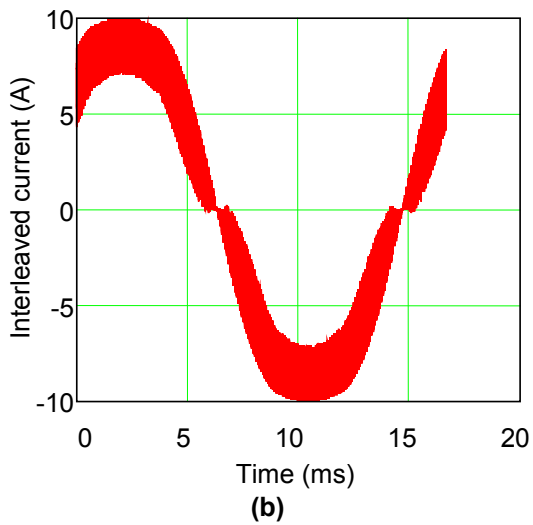
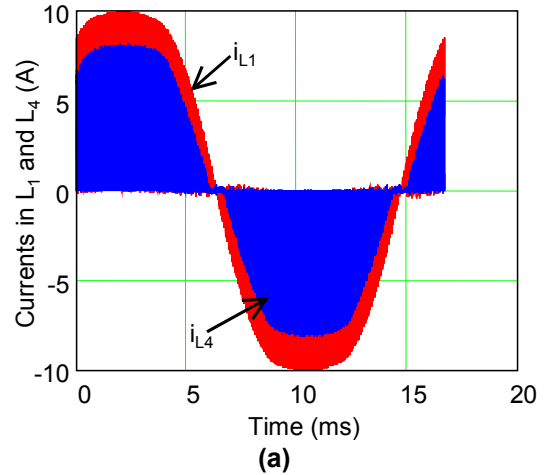
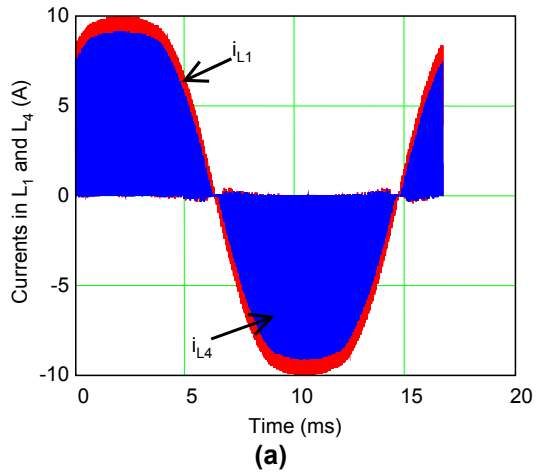


Fig. 5-5. Simulation results for $L_r=2\mu\text{H}$: (a) inductor currents, (b) interleaved current, and (c) amplitude spectrum.

Fig. 5-6. Simulation results for $L_r=5\mu\text{H}$: (a) inductor currents, (b) interleaved current, and (c) amplitude spectrum

The voltage drop across the resonant inductance can be compensated for in order to increase the current in the boost inductors connected through the same path of the auxiliary windings (L_4 , L_5 and L_6). For instance, the transformer turns ratio between the auxiliary and primary windings can be greater than 2:1 in order to reflect a higher voltage across the auxiliary windings to compensate for the voltage drop across the resonant inductance. Another possibility is to reduce the inductance values for L_4 , L_5 and L_6 to increase the boost inductor currents and compensate for the lower voltage reflected across the auxiliary windings. When the resonant inductance is designed to extend the load range for ZVS operation, the solutions above are not so effective for improving the input current ripple cancellation. Thus, the use of the circuit shown in Fig. 5-7 might be a better option. As can be seen, the proposed circuit employs an auxiliary transformer designed with low leakage inductance to drive the auxiliary windings and to bypass the voltage drop across the resonant inductance.

5.3.2. Influence of the Auxiliary Windings on the Transformer Power Rating

The addition of the auxiliary windings alters the primary current and increases the apparent power requirement of the transformer. To show the impact of the auxiliary windings on the increase of the transformer power ratings, consider that the simplified interleaved TL-PS converter shown in Fig. 5-4(b) is designed such that the converter parameters are identical to those used for the non-interleaved TL-PS converter introduced in chapter 4. The parameters used in the comparison are illustrated in Table 4-1. The transformer turns ratio between the auxiliary and the primary windings has been adjusted to 2.1:1 in order to compensate for the voltage drop across the transformer's $2\mu\text{H}$ leakage inductance (no external resonant inductance has been added in the simplified interleaved TL-PS converter).

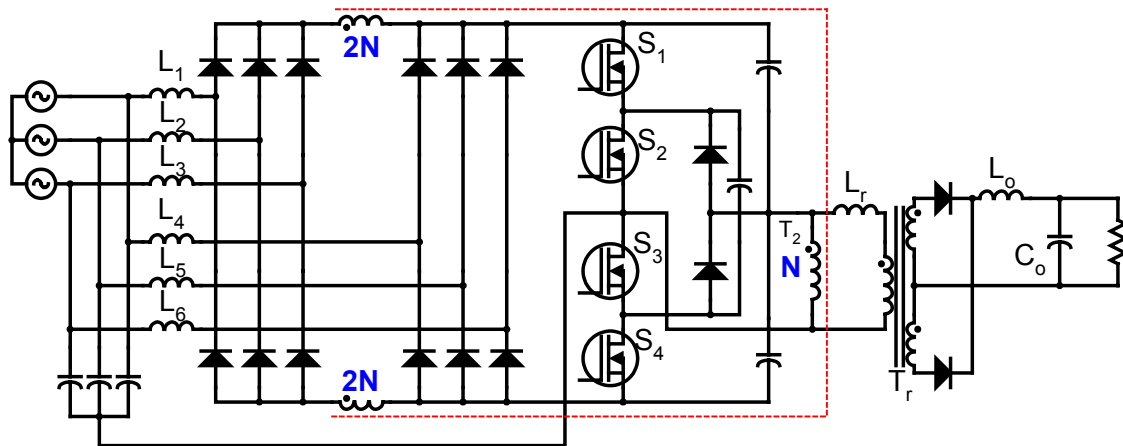


Fig. 5-7. Simplified interleaved circuit using an auxiliary transformer to compensate for a large resonant inductance used to increase the load range with ZVS operation.

Table 5-1. Components used in both interleaved and non-interleaved single-stage TL-PS converters.

Component/Parameter	Non-Interleaved Single-Stage Three-Level Phase-Shift Converter (see Fig. 4-2(b) on page 123)	Simplified Interleaved Single-Stage Three-Level Phase-Shift Converter
Output Power	3kW	3kW
Switching Frequency	50kHz	50kHz
Boost Inductance	110μH	220μH (Each inductance)
Resonant Inductance	11μH	2μH (Transformer leakage inductance)
Output Inductance	5.7μH	5.7μH
Number of Turns	12/3/3	12/3/3(Main windings) + 25/25 (auxiliary windings)
Clamping Capacitance	2μF	2μF

Fig. 5-8 shows the simulation results for both converters under discussion. The simulation was performed at full load and 180V of line-to-neutral input voltage. As shown in Fig. 5-8(a), the insertion of auxiliary windings significantly modifies the shape of the primary current. The two cases present slightly differences in the voltage applied across points A and B. In either case, the magnetizing inductance has been assumed as 1mH.

For the non-interleaved TL-PS converter, the primary RMS current is 16A, the secondary RMS current is 44A, and the power delivered to the output is 3kW. For the simplified interleaved TL-

PS converter, the primary RMS current increases to 26A, the secondary RMS current is still 44A, and the RMS current through the auxiliary windings is 5.8A. The power processed by the transformer used in the simplified interleaved TL-PS converter is 3.85kW (850W are processed in the auxiliary windings), which represents an increase of 28% with respect to the non-interleaved TL-PS converter that delivers the same power to the load.

The same kind of comparison involving the non-interleaved TL-PS converter and the simplified interleaved topology using the auxiliary transformer shown in Fig. 5-7 reveals that the auxiliary transformer processes 1.3kW, which represents 43% of the power processed by the main transformer. Therefore, adding an auxiliary transformer to deal with a large resonant inductance is less advantageous than deriving the auxiliary windings from the main transformer. Evidently, the latter is applicable when there is no resonant inductance in the circuit to increase the load range under which the converter operates with ZVS. In fact, the addition of resonant inductance is not important for increasing the ZVS load range because the energy stored in the boost inductors is sufficient to provide ZVS for a wide load range, which indicates that the most desirable topology for simplifying the interleaving of the input currents is shown in Fig. 5-4(b).

It remains to be assessed how effective the use of auxiliary windings is in reducing the overall converter size, including the DM input filter and boost inductors.

5.3.3. Experimental Results

The proposed simplified interleaved single-stage TL-PS converter has been tested at 3kW and 50kHz of switching frequency. The results that follow were obtained from the simplified interleaved TL-PS converter using a separate auxiliary transformer, even though this variation is

not as good as the simplified interleaved TL-PS converter using the auxiliary windings derived from the main transformer. A separate auxiliary transformer was used because the implementation was relatively easy to do, since the same TL-PS converter implemented in chapter 4 could be used and adapted for this demonstration.

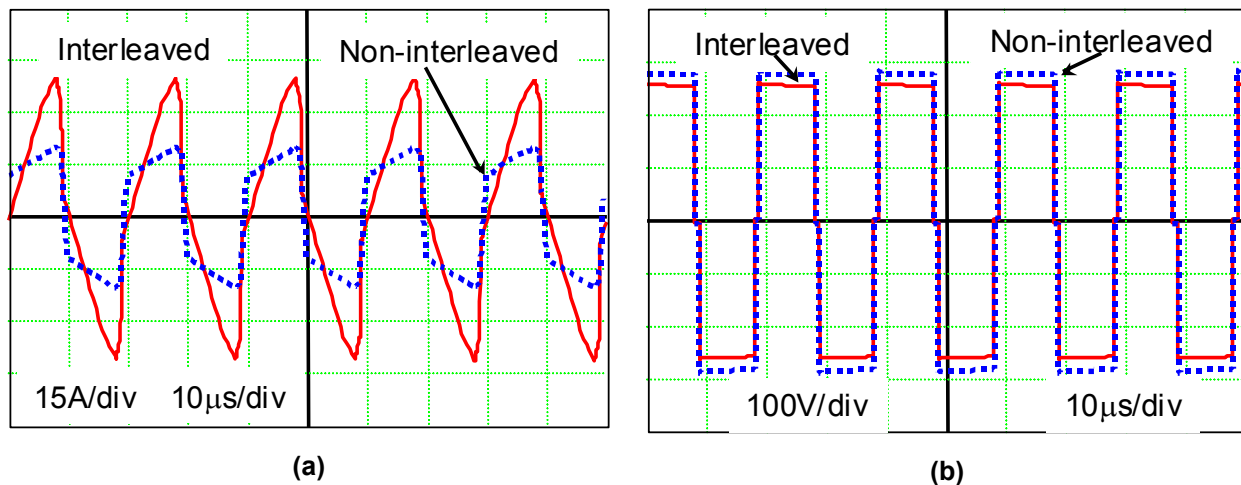


Fig. 5-8. Primary simulated waveforms: (a) transformer current for both simplified interleaved and non-interleaved single-stage TL-PS converter, and (b) voltage applied across points A and B for both converters.

As a result, the parameters and device part count of the circuit shown in Fig. 5-7 are IXFN44N80 for the MOSFETs, RUR30120 for the line rectifiers and clamping diodes, and HFA120MD40D for the output rectifiers. Each bus capacitance consisted of three 1000 μ F/250V electrolytic capacitors connected in series, while the clamping capacitor C_f and the AC capacitors C_a , C_b and C_c were implemented with 2 μ F polypropylene capacitors. The output filter inductance was 5.7 μ H, while the output filter capacitor was 2x4700 μ F/100V, and the resonant inductance has been adjusted to 11 μ H. The auxiliary transformer has been implemented on an E55/21 core using 17 turns of 6x22AWG Cu strand wires in the primary side, and 34 turns 2x20AWG of single-Cu strand wires in the secondary side of the auxiliary transformer. The windings of the auxiliary

transformer have been interleaved to reduce the leakage inductance to $2\mu\text{H}$, while the measured magnetizing inductance was $850\mu\text{H}$.

Fig. 5-9(a) shows the boost inductor currents measured at 3kW and 220V of line-to-neutral input voltage. As can be seen, the current through inductor L_4 is slightly lower than the current through inductor L_1 because of the voltage drop across the $2\mu\text{H}$ leakage inductance of the auxiliary transformer, which has not been compensated for by a turns ratio greater than two to one. Despite the difference between the boost inductor currents, the resulting interleaved current exhibits good input current ripple cancellation.

The amplitude spectrum of the interleaved current is illustrated in Fig. 5-9(b). As can be seen, the harmonic at the switching frequency and other odd harmonics are not fully cancelled out because the interleaving is not ideal, as mentioned above. Although the interleaving is far from the ideal case, the resulting harmonic at the switching frequency is only 0.42A, which represents a fantastic reduction from the 6A measured in the non-interleaved case at the same operating conditions of output power and input phase voltage.

Fig. 5-9(c) shows the interleaved current for three different input phase voltages. A great deal of input current ripple cancellation occurs, but the effectiveness of ripple cancellation deteriorates as the input voltage increases. This problem was expected because the duty cycle is reduced as the input voltage increases, which also reduces the effectiveness of the input current ripple cancellation.

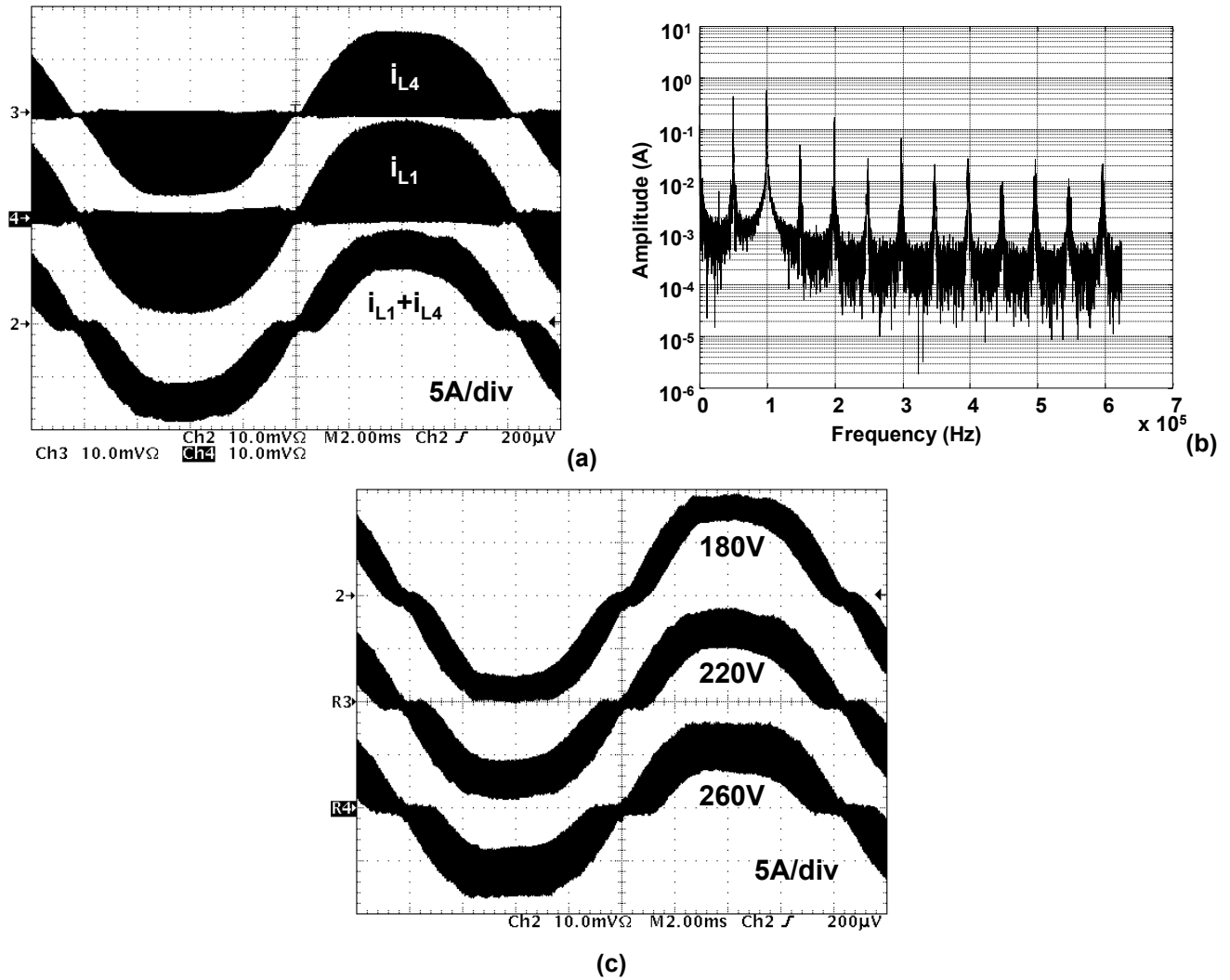


Fig. 5-9. Experimental results obtained at 3kW and 50kHz: (a) boost inductor and interleaved currents at $V_{in}=220V$, (b) amplitude spectrum of the interleaved current at $V_{in}=220V$, and (c) interleaved current measured at three different input voltages.

5.4. DM Input Filter Requirements

This section evaluates the effectiveness of using the simplified interleaved TL-PS rectifier to reduce the size of the DM input filter. Although this evaluation has already been done in the previous chapter, it is repeated here because there is a new element in the spectrum of the interleaved current, which is the noise at the switching frequency that is generated as result of the voltage drop across the transformer leakage inductance.

The amplitude of the high-frequency interleaved current is shown in Fig. 5-10. These curves were obtained by simulating the simplified interleaved converter shown in Fig. 5-4(b), designed for 3kW of output power and 170V to 265V RMS of input voltage variation. No resonant inductance was considered in the simulation, while the leakage inductance was set to $2\mu\text{H}$. Despite interleaving the input currents, one can still observe that the first and all odd harmonics are present in the current spectrum. Therefore, the effect of the switching frequency noise on the input filter size must still be evaluated.

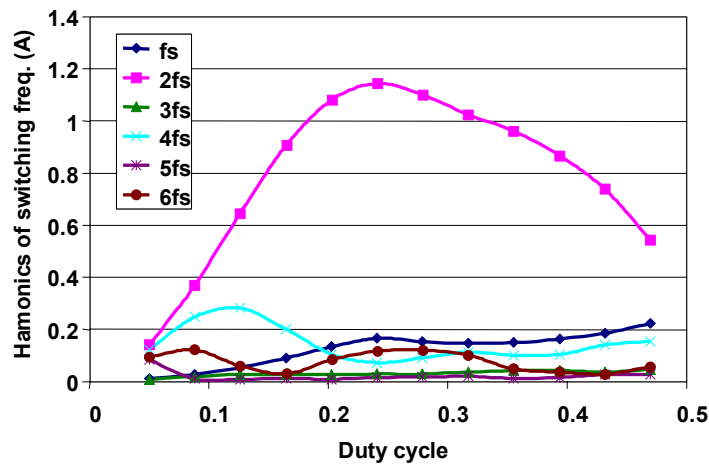


Fig. 5-10. Simulated high-frequency harmonics of the interleaved current.

Fig. 5-11 shows the boost inductances per phase as a function of the switching frequency. For the case of the TL-PS simplified interleaved converter, the boost inductance represented in Fig. 5-11 refers to each of the two inductances connected per phase. As can be noticed, this chapter presents a comparison at 3kW of total power, while the previous chapters compared the converters for 6kW of output power. As a result, the total filter capacitance is reduced $1.9\mu\text{F}$ per phase.

Fig. 5-12 shows the comparison results as a function of the switching frequency. Although the comparison is presented for a switching frequency of 40kHz to 200kHz, attention should be

focused on the switching frequencies between 40kHz and 75kHz instead. The reason for limiting the analysis within this switching frequency range is because the efficiency of single-stage converters at higher switching frequencies is very low. The network of the filter used for the comparison is the same as that used in the previous chapters.

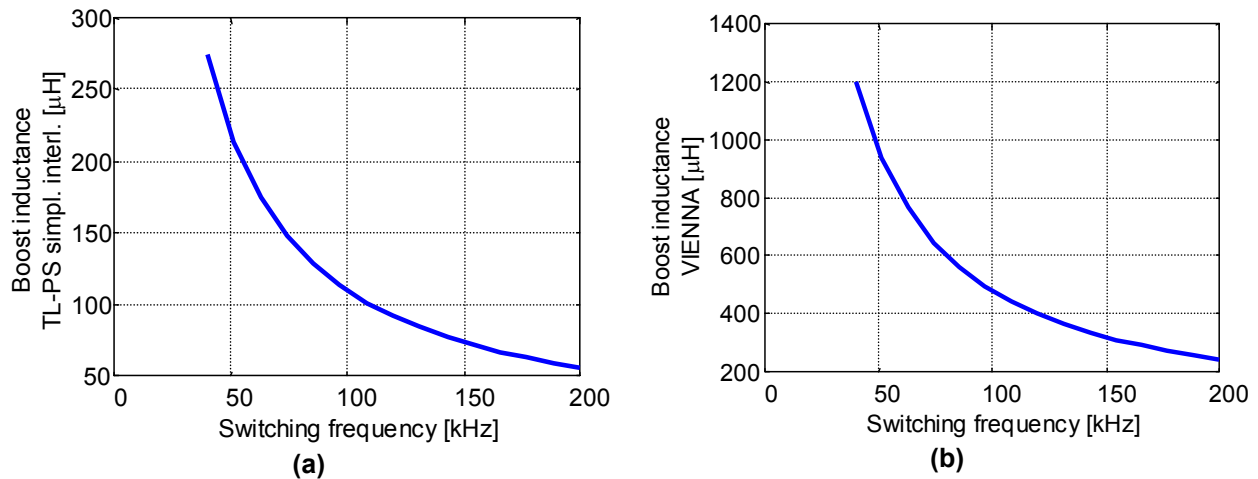


Fig. 5-11. Boost inductance vs. frequency: (a) 3kW TL-PS simplified interleaved converter and (b) 3kW VIENNA rectifier.

Fig. 5-12(a) and Fig. 5-12(b) show the filter inductances L_1 and L_3 as a function of switching frequency for the CISPR 22 Class B standard. Clearly, the VIENNA is far better than the interleaved system in terms of filtering requirements below 150kHz. Although the VIENNA rectifier requires less filtering than the simplified interleaved converter, the curves show that below 150kHz, the switching frequency has no effect on reducing the minimum inductances of the filters. The estimated weight of the filter inductor per phase is shown in Fig. 5-12(c) and Fig. 5-12(d). As can be seen, it follows the same trends of the inductance values. From these figures, the benefit of interleaving converters in reducing the size of the DM input filter is not clear. However, as shown in Fig. 5-12(e) and Fig. 5-12(f), the combined weight of the equivalent boost and filter inductors per phase is reduced to below 75kHz for the simplified interleaved TL-PS single-stage converter.

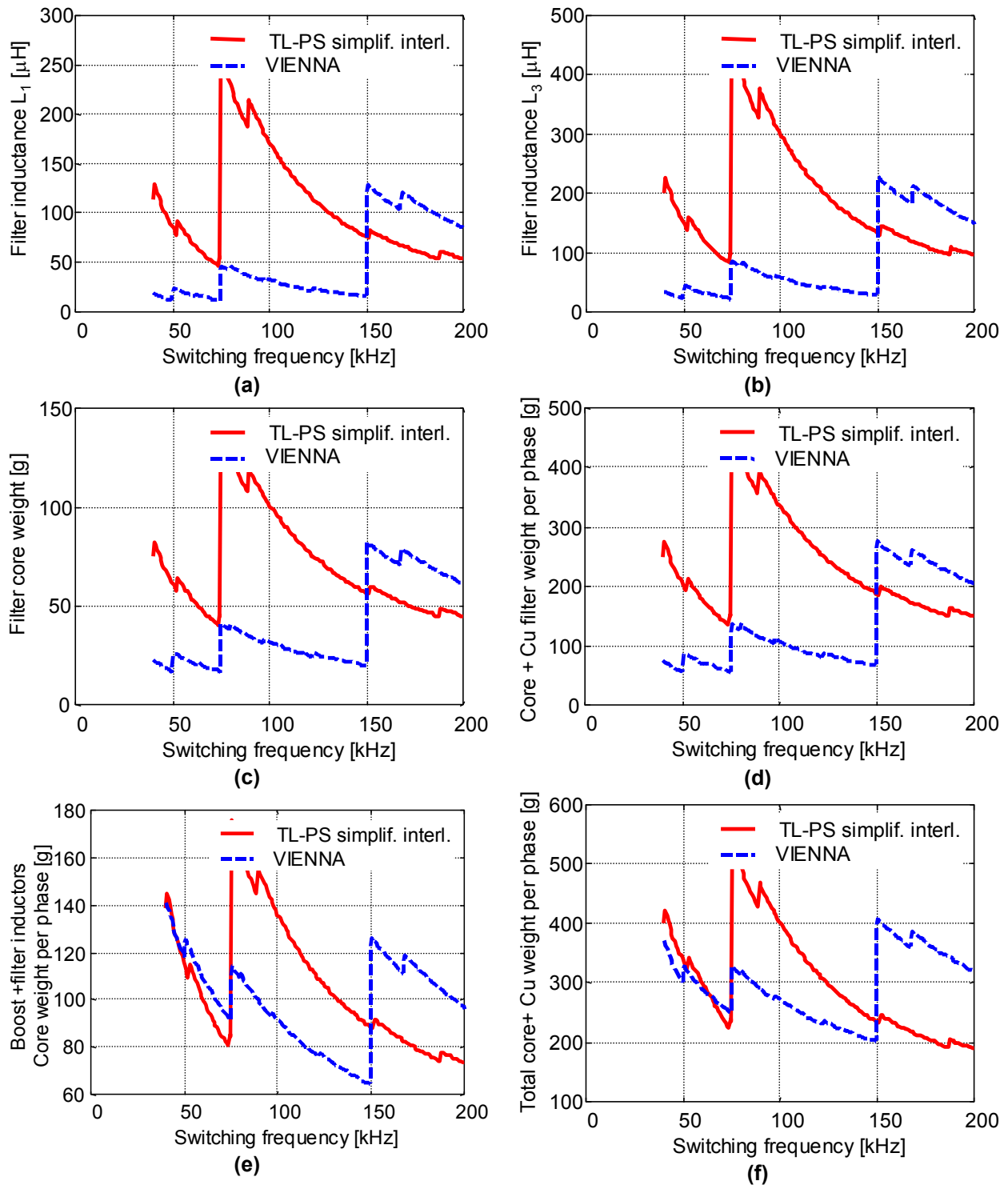


Fig. 5-12. Results of comparison: (a) filter inductance L_1 , (b) filter inductance L_3 , (c) filter core weight, (d) combined filter core and winding weight per phase, (e) core weight of filter and boost inductors per phase, and (f) overall filter and boost inductors weight per phase (core + winding Cu).

5.5. Conclusion

A simplified interleaving technique was presented in this chapter. Based on the use of magnetic switches, this technique is implemented without doubling the switching power stage. The magnetic switches used in the topology are realized with auxiliary windings linked to the main transformer. As demonstrated, the number of turns in each auxiliary winding must be at least twice the primary number of turns to provide input current ripple cancellation.

Each input phase is connected to two boost inductors. The switching power stage and the magnetic switches produce two high-frequency voltages that are 180° apart in a switching period. As a result of these two phase-shifted high-frequency voltages, the two boost inductor currents connected to the same phase are also phase-shifted by 180° , providing input current ripple cancellation.

The influence of the resonant inductance on the input current ripple cancellation has also been presented. The resonant inductance is used to increase the load range under which the converter operates with ZVS. However, the effect of the resonant inductance is to generate a voltage drop across the voltage imposed by the magnetic switches on the boost inductors. As a result, the input current ripple cancellation effectiveness is reduced, and there is difference between the levels of each boost inductor connected to the same phase.

The effect of the resonant inductance in increasing the load range for ZVS is not so important because the input boost inductor currents are able to contribute with much more energy to the ZVS operation than the resonant inductance itself. As a result, the resonant inductance can be eliminated such that the only inductance connected in series with the transformer is the leakage inductance, reducing the effect of the voltage drop across the auxiliary windings, and

consequently improving the input current ripple cancellation. As demonstrated, the addition of auxiliary windings increases the power processed by the transformer by 28% as compared with the non-interleaved TL-PS single-stage converter.

Regarding the input filter size, a comparison has been provided between the simplified interleaved converter and the VIENNA rectifier, which was redesigned for an output power of 3kW. For the CISPR 22 Class B standard, the VIENNA rectifier results in smaller filter size as compared to the simplified interleaved converter. However, when the weight of the filter inductors is combined with the weight of the boost inductor, the simplified interleaved converter results in a smaller overall size as compared to the VIENNA rectifier. The comparison is meaningful for the switching frequency range between 40kHz and 75kHz, since above this switching frequency the efficiency of the single-stage converter is questionable.

6. General Conclusion

Distributed power systems are widely used to supply energy to modern telecommunication systems, mainframe computers and servers. The major benefits of DPSs are the ability to supply large systems, while increasing reliability, system redundancy and availability. The flexibility to expand the system capacity as the load requirements increase and the ability to quickly replace faulty modules are additional advantages of the DPSs. The front-end converters, built to provide PFC function and to regulate the DC distribution bus voltage, are the DPS building blocks.

The PFC function is required in the European Community because of the harmonic standards, whereas in the U.S. the market itself has imposed this type of feature to the front-end converters for DPS applications. Despite the requirements and the market demands, the end user is not willing to pay for any extra cost that has to be added in order to guarantee the PFC function. As a result, there are many reasons for developing research on low-cost PFC circuits used for high-power DPS applications.

Based on the previous discussion, this dissertation presented simple and low-cost solutions for three-phase PFC used in DPS applications. The main purpose of this dissertation was to develop 3kW to 6kW PFC circuits, while achieving the following features: (1) reduced complexity and (2) reduced cost with reasonable performance.

CHAPTER 1 presented an overview of the main solutions for front-end PFC converters. From that discussion, two circuits were selected as the benchmark circuits: (1) the CCM boost and (2) the VIENNA rectifiers. These circuits are the most widely industry used solutions to provide

PFC function to front-end converters. All the other circuits presented in this dissertation were compared against the benchmark circuits.

CHAPTER 2 presented a two-stage front-end converter using a single-switch three-phase DCM boost rectifier in the PFC stage. The advantages and drawbacks were analyzed, while improvements were implemented to increase the performance of the single-switch three-phase DCM boost rectifier, such as the harmonic injection method used to reduce the THD of the input currents. When the harmonic injection method was used, 8kW could be extracted from the single-switch DCM boost rectifier, while still complying with the IEC 61000-3-2 harmonic standard without increasing the intermediate bus voltage beyond 800V. Because the intermediate bus voltage was 800V, IGBTs operating at 40kHz were used in the implementation, whereas a ZCT soft-switching circuit was implemented to allow soft turn-off for the main IGBTs. The DCM operation of the single-switch boost rectifier requires large filters to attenuate the high input current ripple. Therefore, interleaving the single-switch DCM boost rectifiers was explored as an alternative method to reduce the filtering requirements. Considering the VDE 0871 Class B EMI standard, the interleaving of two single-switch DCM boost rectifiers reduced the filtering requirements to a level similar to that of the CCM boost and VIENNA rectifiers. On the other hand, the reduction in filtering requirement due to interleaving is not clear when the CISPR 22 is taken into account. To demonstrate the advantages of interleaving DCM boost rectifiers under the CISPR 22 EMI standard, both filter and boost inductors should be combined in the overall magnetic size comparison. Combining the sizes of boost and filter inductors demonstrated that interleaving is quite advantageous in reducing the requirements for magnetic devices, especially in the switching frequency range from 50kHz to 75kHz, as well as above 150kHz. Including the

DM filter, the overall efficiency of the interleaved single-switch DCM boost rectifiers designed for 6kW was 95.8% at 220V line-to-neutral input voltage.

A two-stage front-end converter was developed in chapter 2 to supply 6kW of output power to a 48V DC bus. Because the intermediate bus voltage provided by the interleaved PFC system was 800V, the front-end DC/DC converter was implemented with a ZVZCS three-level converter operated at 100kHz. The resulting system combines simplicity and performance in a compact two-stage front-end converter. The overall system efficiency, including the EMI filter, was 90.5% at full load and nominal input voltage (220V line-to-neutral input voltage).

The second system described in CHAPTER 3 was also a two-stage front-end converter in which the PFC stage was implemented with a two-switch three-level DCM boost rectifier. The motivation for this particular work was to use power MOSFETs in the PFC stage. The use of MOSFETs allows the switching frequency to be increased in order to reduce the size of the input filter. The two-switch three-level DCM boost rectifier resulted in 8.8% THD at 220V input line-to-neutral voltage. The harmonic injection method had a major impact in reducing the THD to below 10% over the entire input voltage variation. Using 600V power MOSFETs with low R_{ds-on} achieved a PFC efficiency of 97.4% at a switching frequency of 40kHz and 96.4% at 70kHz. Interleaving was also explored as an alternative way to decrease the input current ripple, and consequently the filtering effort. Under the CISPR 22 EMI standard, two-channel interleaved two-switch three-level DCM boost rectifiers had a great impact on the overall size reduction of the boost and filter inductors. From the point of view of reduced overall boost and filter inductor sizes, the best switching frequency range to design the interleaved two-switch DCM boost rectifiers was between 50kHz and 75kHz, as well as above 150kHz.

The two-stage front-end converter obtained with the interleaved two-switch three-level DCM boost rectifiers and the DC/DC three-level ZVZCS converter yielded an efficiency of 92.1% when the PFC stage was operated at 40kHz, and 91.3% when operated at 70kHz. As a result, the two-switch three-level DCM boost rectifier outperforms its single-switch counterpart in terms of both efficiency and THD. Thus, the two-switch three-level DCM boost rectifier makes the best cost tradeoff PFC option for DPS front-end converters. The two-stage front-end converter approach is quite suitable for telecom applications because the DC/DC converter can provide fast regulation and easier compliance with output ripple limits and noise, such as the psophometric noise.

Power modules for mainframe computers and server applications are usually designed for less than 1.2kW, but with the increasing demand for computer applications, the power requirements are likely to increase in the future. To further simplify and lower the cost of three-phase front-end converters, the second part of this dissertation was dedicated to single-stage three-phase front-end converters operated at zero-voltage switching. The first single-stage module presented in CHAPTER 4 was based on the integration of a two-switch three-level DCM boost rectifier with a three-level phase-shift ZVS DC/DC converter. The resulting single-stage three-level phase-shift converter presented a THD lower than 7% at full load and 87% of overall efficiency, including the input filter. To reduce the conduction loss, another single-stage front-end converter was proposed, based on the functional integration of a two-switch three-level DCM boost rectifier and a three-level DC/DC asymmetrical converter. This reduced the conduction loss by 50% when compared to the single-stage three-level phase-shift module. By reducing the

conduction loss, the asymmetrical front-end converter improved the overall efficiency to 89% at 50kHz.

Despite improving the overall efficiency, the single-stage three-level asymmetrical topology presented higher THD as compared to the single-stage three-level phase-shift converter. The other drawback presented by the asymmetrical topology was the voltage across the DC blocking capacitor, requiring the use of either polypropylene or film capacitors. The transformer also needs more turns to compensate for the DC magnetizing current that builds up during the asymmetrical operation of the circuit. As a result, the three-level phase-shift converter is still the preferred single-stage topology, as it presents a low-cost potential use in mainframe computers and servers. For telecom applications, it was verified that single-stage front-end converters also provide low levels of psophometric noise in the output voltage. Both single-stage topologies discussed in chapter 4 experience a voltage stress across the intermediate bus voltage. However, the three-level topologies used to implement the single-stage converters help alleviate the voltage applied across the power switches. In general, the performance of a two-stage front-end converter is superior when compared to single-stage topologies. However, cost has driven the development of single-stage converters. In many cases, customers are willing to trade off performance for lower-cost solutions.

Chapter 4 also explored the interleaving of single-stage AC/DC converters. For the CISPR 22 Class B EMI standard, it was demonstrated that the combined sizes of boost and filter inductors are reduced as compared to the requirements of the VIENNA rectifier. The best practical switching frequency range for the design of interleaved single-stage AC/DC converters is between 50kHz and 75kHz.

Interleaving single-stage front-end converters is an alternative way to reduce filtering requirements. However, interleaving single-stage rectifiers must rely on doubling the switching power stages. To overcome this problem, CHAPTER 5 proposed a simplified interleaving approach using the single-switch three-level phase-shift converter. The technique implemented in chapter 5, combined the power stage and magnetic switches to produce two high-frequency voltages phase-shifted by 180° . As a result of these two phase-shifted high-frequency voltages, the two boost inductor currents connected to the same phase were also phase-shifted by 180° , thus providing input current ripple cancellation. The effect of the resonant inductance on the input current ripple cancellation was investigated, and measurements to correct the problem were presented. Among the correction measures are the elimination of the resonant inductance from the circuit or the use of a separate auxiliary transformer to implement the auxiliary windings. As demonstrated, the power processed by the transformer with auxiliary windings increases by 28%, while using a separated transformer requires it to be designed to withstand 43% of the output power. Regarding the input filter size, a comparison for the CISPR 22 EMI standard demonstrated that the VIENNA rectifier resulted in smaller filter size, as compared to the simplified interleaved converter. However, when the weight of the filter inductors is combined with the weight of the boost inductors, the simplified interleaved converter results in smaller overall magnetic size. The comparison is meaningful for the switching frequency range from 40kHz to 75kHz, since above this switching frequency the efficiency of the single-stage converter is questionable. Because of the simplicity of canceling the input current ripple and the benefits of interleaving, the simplified interleaved single-stage converter is indeed a potential low-cost candidate for mainframe computers, server, and even telecom applications.

Appendix I – Inductor Design

Introduction

Kool M μ powder cores are naturally suited to the design of designing inductors because they provide a higher energy storage capability than gapped ferrite cores of the same size and effective permeability. The high flux density and low core losses make Kool M μ powder cores quite suitable for PFC applications. Where a significant current ripple may contribute to heat rise, such as in DCM rectifiers, Kool M μ powder cores will present superior performance as compared to iron powder cores as well. The following paragraphs are dedicated to describing the procedure used to design the boost and filter inductors for the comparisons of the various rectifiers presented throughout this work.

Design Variables and Constraints

The first step for designing inductors is to define the core geometry, as illustrated in Fig. I- 1. In the following formulae, the variable OD stands for outside diameter, ID for inner diameter, and HT for core height. The inductor design yields continuous results, which means that OD, ID and HT can assume any value within a certain range, which is limited by the following form-factor constants:

$$(I-1) \quad \begin{aligned} k_d &= \frac{OD}{ID} \\ k_h &= \frac{HT}{OD - ID} \end{aligned} ,$$

where $k_d=1.6$ and $k_h=0.85$. These form-factor constants have not been arbitrarily chosen, but instead they have been based on the average form-factor constants obtained from commercial cores [58].

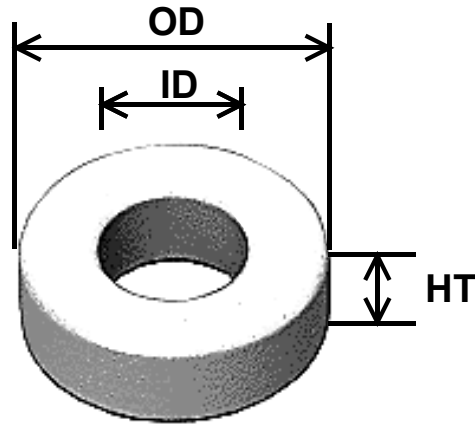


Fig. I- 1. Core geometry.

Several constraints were assumed for the design of the inductors, such as maximum current density $J_{max}=450A/cm^2$ and maximum core temperature rise $\Delta T=50^\circ C$. The 60μ core material has been chosen for the design of the inductors because it provides high saturation flux, while still maintaining a reasonable permeability. Fig. I- 2 shows the flux density and initial permeability for the 60μ core material.

The design objective is to determine the core geometry in order to calculate core and winding weights for the purpose of comparison between the various circuits discussed in the dissertation. A simple computer algorithm has been developed to design the inductors, which takes into account core and winding losses. The skin effect in the conductors has been considered in the calculations, while any proximity effect has been ignored. The following paragraphs describe the procedure used to design the inductors.

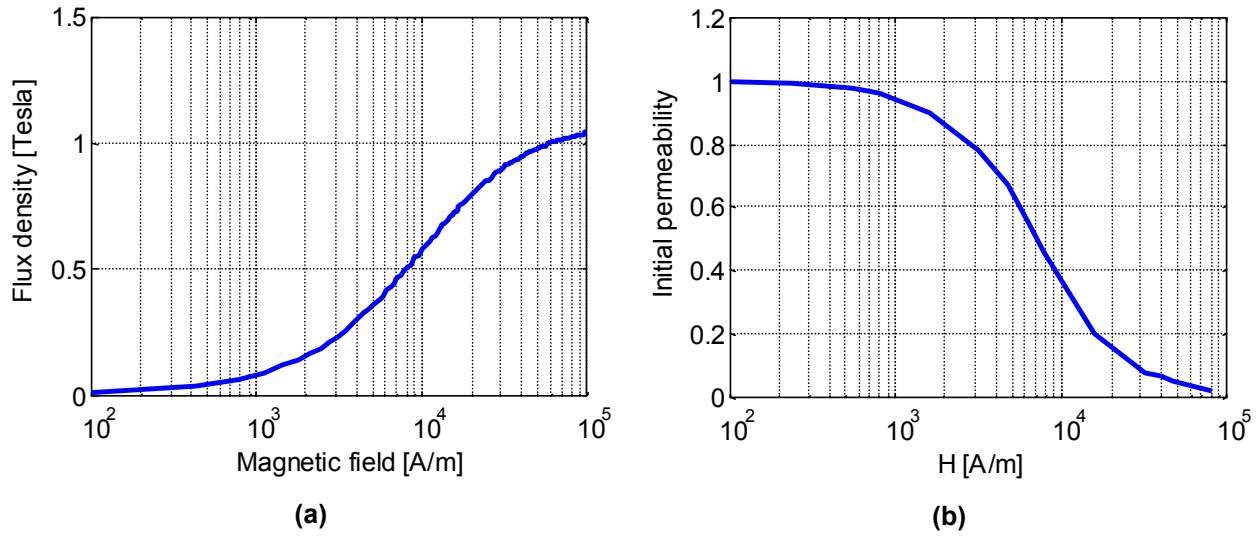


Fig. I- 2. (a) Flux density and (b) initial permeability as a function of the magnetic field for 60μ core material.

Step 1- Core Area Product

The first design step is to determine the core area product according to the well-known relationship described below:

$$(I-2) \quad A_p = \frac{L I_{rms} I_{pk}}{k_w B_{pk} J_{max}},$$

where I_{rms} is the RMS current through the inductor, I_{pk} is the inductor peak current, $k_w=0.4$ is the window factor utilization, B_{pk} is the peak flux density at the peak current, and J_{max} is the maximum winding current density.

For the initial design guess, the magnetic field at the peak current is set to 135 Oe⁵, while the flux density can be determined with the expression below:

⁵ Multiply Oe by $k_1=79.577$ to obtain A/m.

$$(I-3) \quad B = \underbrace{60 \mu_{ini} \mu_o}_{\mu} H ,$$

where μ_{ini} is the initial permeability obtained from Fig. I- 2(b) for a given H, and $\mu_o=4\pi \times 10^{-7}$ H/m is the air permeability.

Step 2- Core Geometry

The core geometry can then be determined from the area product as follows:

$$(I-4) \quad \begin{aligned} HT &= \frac{2^{3/4}}{\pi} \left[A_p k_h^3 (k_d^2 - 2k_d + 1) \pi^3 \right]^{1/4} \\ OD &= \frac{k_d HT}{k_h (k_d - 1)} \\ ID &= \frac{HT}{k_h (k_d - 1)} \end{aligned} .$$

The core volume and magnetic length can be determined with the help of the following relationships:

$$(I-5) \quad Vol_{core} = HT \left[\pi \left(\frac{OD}{2} \right)^2 - \pi \left(\frac{ID}{2} \right)^2 \right], \text{ and}$$

$$(I-6) \quad l_m = \pi \left(\frac{OD + ID}{2} \right).$$

Step 3- Number of Turns

The number of turns is determined by

$$(I-7) \quad N = \text{floor} \left(\frac{H l_m}{I_{pk}} \right),$$

where the function “floor” rounds down the number of turns to the nearest integer number. Because of the approximation above, one must correct the final magnetic field and flux density experienced by the core, as follows:

$$(I-8) \quad \begin{aligned} H_c &= \frac{NI_{pk}}{l_m} \\ B_c &= \underbrace{60 \mu_{ini} \mu_o}_{\mu_c} H_c \end{aligned}$$

Step 4- Verification of Window Utilization Factor

To determine whether or not the winding can be fitted inside the core window, one must determine the cross-section area of Cu wire needed to wind the core. The Cu wire needed for each inductor can be determined by

$$(I-9) \quad S_{Cu-wire} = \frac{I_{rms}}{J_{max}},$$

where $S_{Cu-wire}$ represents the area of a single-strand Cu wire required to withstand the RMS current of the inductor. For the DCM boost inductor, the skin effect must be take into account by calculating the skin depth according to

$$(I-10) \quad \delta_{(cm)} = \frac{7.5}{\sqrt{f_s}}.$$

When the skin depth is greater than the radius of the Cu wire, it is necessary to parallel several single-strand Cu wires to obtain the required RMS current capability, while limiting the radius of each single-strand Cu wire so that it is lower than the skin depth. Once the Cu wire has been chosen, one can determine the core window area occupied by the winding, which is given by

$$(I-11) \quad S_{Cu-winding} = N S_{Cu-wire} n_{wire},$$

where N is the number of turns, $S_{Cu-wire}$ is the cross-section area of a single-strand Cu wire, and n_{wire} is the number of wires in parallel to satisfy the skin depth requirements. If the ratio between the total Cu area and the window area is greater than k_w (window utilization factor), then the core area product must be increased, and the design must restart at step 2. The incremental increase for A_p implemented in the computer algorithm was 1%.

Step 5- Core Loss Estimation

The core loss density is determined with the help of the Steinmetz equation, which is empirically written as

$$(I-12) \quad P_w = \Delta B_{(kGauss)}^2 f_{s(kHz)}^{1.46}.$$

The expression above was empirically derived under the consideration of a sinusoidal excitation. As a result, this relationship can be directly used to design the filter inductors. For the CCM and DCM boost inductors, however, the current ripple plays an important role in the core loss, and for this reason must be taken into account.

Fig. I- 3 shows the boost inductor current for a given operating point. It is assumed that the core is operated in the non-saturation region of the BxH curve. A Fourier expansion of the arbitrary ripple current can be obtained for each switching period, and thus the core loss density for that switching period can be determined by calculating the loss density for each harmonic, and by superimposing the various harmonics yields on the total loss density for that switching period [89] [90]. The total average core loss density over the line period is obtained by averaging the

core loss calculated for every switching cycle. The loss density caused by the line frequency component can also be superimposed onto the high-frequency ripple loss density. However, this loss component is much lower than the loss caused by the ripple current. This method used to determine the core loss density holds for linear systems only, and is invalid for non-linear magnetic materials [91] [92]. After determining the core loss density using this procedure, the power loss of the core is given by

$$P_{core} = P_w Vol_{core},$$

where P_w is the loss density and Vol_{core} is the core volume determined from (I-5). The same procedure can be also applied to DCM boost inductors.

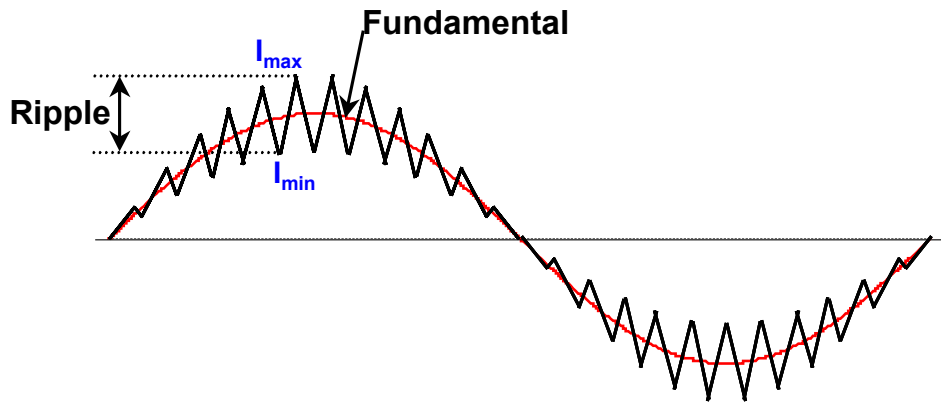


Fig. I- 3. CCM boost inductor current.

Step 6- Winding Loss Estimation

The Cu loss is related to the winding resistance, which is in turn related to the total length of Cu wire used in the winding. A simple representation of the winding built around the core is depicted in Fig. I- 4(a). In order to determine the total Cu wire length, one must first calculate first the average turn length.

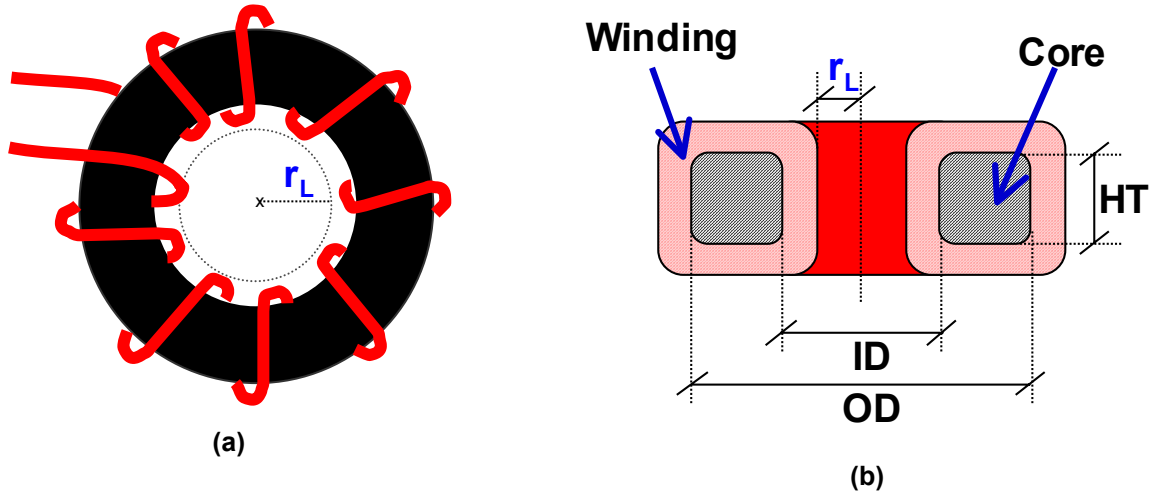


Fig. I- 4. (a) Winding dimensions and (b) cross-sectional view of core and Cu winding.

Fig. I- 4(b) shows a cross-section view of the core and winding. As can be seen, the internal radius that is not filled up with Cu can be determined as

$$(I-13) \quad r_L = \sqrt{\frac{A_w - N S_{Cu-wire} n_{wire}}{\pi}},$$

$$A_w = \pi \left(\frac{ID}{2} \right)^2,$$

where A_w is the is the core window area.

The average turn length can be easily obtained from the inductor cross-section view shown in Fig. I- 4(b), as follows:

$$(I-14) \quad l_t = 2 \left(HT + \frac{ID}{2} - r_L \right) + 2 \left(\frac{OD - ID}{2} + \frac{ID}{2} - r_L \right).$$

The following relationship can then be used to determine the winding loss:

$$(I-15) \quad P_{Cu} = \frac{R_{\Omega/m} l_t N}{n_{wire}} I_{rms}^2,$$

where $R_{\Omega/m}$ is the resistance per length unit of the single-strand Cu wire selected to withstand the RMS current and to comply with the skin depth constraint.

Step 7- Temperature Rise

The temperature rise in a wound core depends on the Cu and core losses, as well as on the total exposed surface area of the inductor [58]. It can be determined with the empirical expression described below:

$$(I-16) \quad \Delta T_{oC} = \left[\frac{(P_{Cu} + P_{core})10^3}{S_{total}} \right]^{0.833},$$

where S_{total} is the total surface area for heat transfer given in cm^2 . S_{total} can be determined by the following relationship:

$$(I-17) \quad S_{total} = \frac{\pi}{2}(OD + ID)(OD + 3ID - 8r_L + 2HT).$$

The calculation of ΔT is a design checkpoint, as shown in Fig. I- 5. If ΔT is lower than the constrained temperature rise, then the design procedure can continue. However, if ΔT exceeds the specified temperature rise, then one must determine which loss component is higher so that either H_c or J_{max} can be reduced to decrease ΔT .

Step 8- Weight Calculation

To calculate both core and Cu weights, the total volume of the assembly must be determined from Fig. I- 4(b) as follows:

$$(I-18) \quad V_{total} = \pi \left[\frac{OD + 2 \left(\frac{ID}{2} - r_L \right)}{2} \right]^2 \left[HT + 2 \left(\frac{ID}{2} - r_L \right) \right] - \pi r_L^2 \left[HT + 2 \left(\frac{ID}{2} - r_L \right) \right].$$

The core volume can be calculated from (I-5), while the Cu volume is simply given by the difference ($V_{total} - Vol_{core}$).

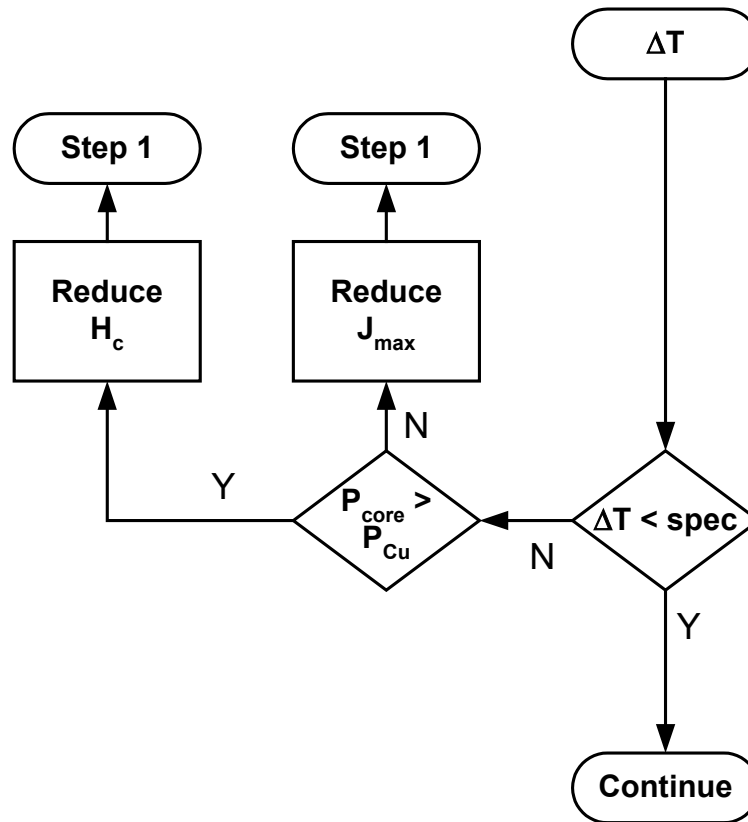


Fig. I- 5. Flowchart for the temperature rise design checkpoint.

For the weight calculation, the Kool M μ core density is $D_{core}=5781\text{Kg/m}^3$, while the Cu density is $D_{Cu}=8290\text{Kg/m}^3$. The following expressions can be used to determine the core and Cu weights.

$$(I-19) \quad \begin{aligned} W_{core} &= D_{core} Vol_{core} \\ W_{Cu} &= D_{Cu} (V_{total} - Vol_{core}) \end{aligned}$$

Appendix II - Calculation of Filter Parameters

Introduction

This appendix describes how the DM filter parameters were designed for the various PFC circuits discussed throughout the dissertation. The design guidelines are based on the results reported in previous work [56] [57].

The basic configuration of a PFC circuit and filter can be seen in Fig. II- 1. Using the phasor diagram, the PFC circuit produces a current i_a in phase with the voltage v_a . Because the voltage drop across L is very small at the line frequency, one can assume that $v_a = v_{in}$. The voltage v_a imposes a 90° -leading current through C , as shown in the phasor diagram. The phasor diagram can also be used to derive the following relationship to determine θ :

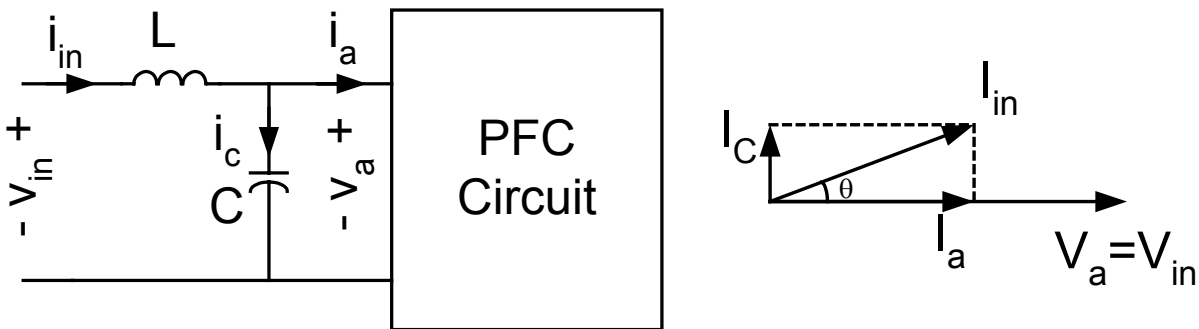


Fig. II- 1. Displacement factor.

$$(II-1) \quad \theta = \tan^{-1} \left(\frac{2\pi f_r C V_{pk}}{I_{pk}} \right),$$

where I_{pk} is the fundamental peak of the current i_a , and V_{pk} is the peak input phase voltage. From (II-1), the maximum filter capacitance is determined as follows:

$$(II-2) \quad C_{\max} = \frac{I_{pk-\min}}{2f_r V_{pk-high}} \tan(\cos^{-1} IDF),$$

where IDF is the input displacement factor, which is measured as the cosine of the phase angle between the voltage v_{in} and current i_{in} , $I_{pk-\min}$ is the peak value of the current i_a at minimum or partial load, and $V_{pk-high}$ is the high-line peak input voltage. For the various PFC circuits discussed in the dissertation, the displacement factor was assumed to be 0.95, measured at high-line input voltage and 15% of full load. For the designs discussed in the dissertation, the full power per phase was 2kW, while the high-line input phase voltage was 265V RMS. As a result, the maximum filter capacitance from (II-2) is approximately 3.8 μ F per phase. For a multiple-stage filter, the total capacitance is the parallel combination of the various capacitances required in each stage.

Besides the requirements for displacement factor, the filter designed for PFC applications must not interact with the closed-loop system of the PFC circuit [88]. The latter requirement is not an issue for DCM rectifiers because the crossover frequency for these converters is well below the resonant frequency of the filter poles.

EMI Filter Design Procedure

It is important to obtain small filter component values and sizes. As a result, the filter corner frequency must be close to the frequency of the noise to be attenuated, which requires the filter to have a very steep attenuation characteristic near the noise frequency. Only high-order filters are able to realize this type of characteristic while maintaining a reasonable size and meeting PFC requirements. One type of filter that is known to provide such characteristic is the Cauer-Chebyshev (CC) filter, also known as elliptic-integral filter [57]. A two-stage CC filter with

normalized parameters is shown in Fig. II- 2. The normalized filter parameters are given in previous work [57] (pages 200-201), and are shown in Table II- 1.

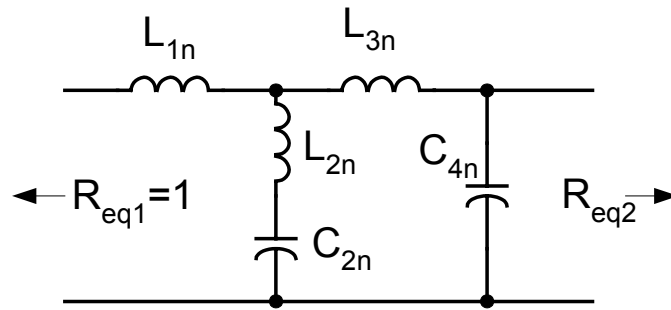
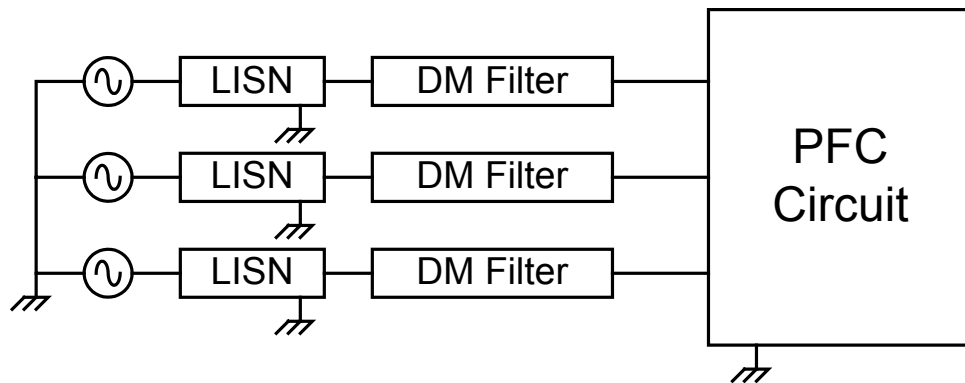
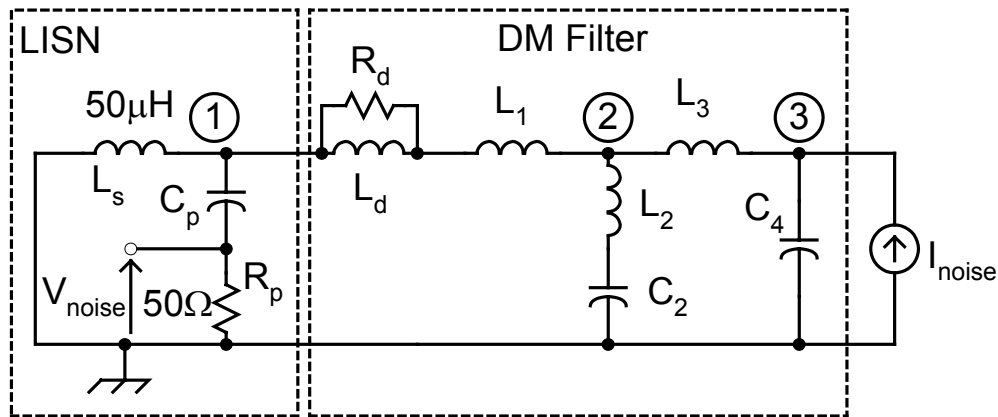


Fig. II- 2. Cauer-Chebyshev (CC) filter.



(a)



(b)

Fig. II- 3. (a) Three-phase setup and (b) equivalent circuit per phase.

The simulation block diagram for the three-phase equipment under test using the DM filter and LISN is shown in Fig. II- 3(a). As can be seen, the neutral point is grounded, while three single-phase LISNs are used to measure the noise. The calculation of the filter parameters is performed per phase, using the equivalent circuit illustrated in Fig. II- 3(b). The parameters R_d and L_d are the high-frequency damping resistor and the low-frequency current bypass inductor, respectively. In the design of the input filter for all converters described throughout the dissertation, a $6\text{dB}\mu\text{V}$ margin was used, and no common-mode noise was ever considered in the calculation. The following paragraphs describe a computer algorithm used to design the input filter parameters.

Step 1- EMI Standard

Define the standard to be used for the design of the input filter. As can be seen throughout this dissertation, the VDE 0871 and the CISPR 22, both Class B, have been selected to design and compare the DM filter for the various PFC circuits.

Step 2- Current Ripple

Determine the worst-case scenario for the input current ripple generated by the converter under consideration. Determine the spectrum of the worst-case input current ripple to be attenuated by the DM filter.

Step 3- Normalized Filter Parameters

Choose the normalized filter parameters from Table II- 1. The design should start with the filter parameters that provide the lowest attenuation given in Table II- 1.

Step 4- Denormalizing the Filter Parameters

There are several sub-steps in the denormalization of the filter parameters.

a) Reference Frequency

$$(II-3) \quad \omega_r = 0.8 \frac{2\pi f_{noise}}{\Omega_s},$$

where Ω_s is the normalized frequency from Table II- 1 and f_{noise} is the frequency of the noise to be attenuated. The reference frequency is chosen to be below the noise frequency in order to reduce the effect of the filter parameter variations that occur due to temperature, tolerance, aging, etc., thus guaranteeing that the noise frequency will stay within the filter stop-band region.

b) Determine the High-Frequency Damping Resistor

$$(II-4) \quad R_d = \frac{C_{2n} + C_{4n}}{\omega_r C_{max}},$$

where C_{max} is obtained from (II-2) at high line and 15% of full load.

c) Denormalize the Filter Inductances

$$(II-5) \quad L_i = \frac{L_{in} R_d}{\omega_r}, \quad \text{where } i = 1, 2 \text{ and } 3.$$

d) Denormalize the Filter Capacitances

$$(II-6) \quad C_k = \frac{L_{kn} R_d}{\omega_r}, \quad \text{where } k = 2 \text{ and } 4.$$

e) Choose the Low-Frequency Current Bypass Inductance L_d

The inductor L_d solves the dissipation problem in the damping resistor R_d by providing an alternative path for the line-frequency current. For the parallel network $R_d//L_d$ to be effective, the corner frequency $f_d=R_d/(2\pi L_d)$ must be lower than the lowest filter frequency pole. As a result, L_d is chosen to be equal to L_1 for all cases designed throughout the dissertation.

Step 5- Design Verification

In this step, the design is theoretically verified by using the equivalent network shown in Fig. II- 3(b). The node equations for the system shown in Fig. II- 3(b) are given below:

$$(II-7) \quad \begin{bmatrix} 0 \\ 0 \\ I_{noise} \end{bmatrix} = \begin{bmatrix} \frac{1}{sL_s} + \frac{1}{R_p + \frac{1}{sC_p}} + \frac{1}{sL_1 + \frac{R_d sL_d}{R_d + sL_d}} & -\frac{1}{sL_1 + \frac{R_d sL_d}{R_d + sL_d}} & 0 \\ -\frac{1}{sL_1 + \frac{R_d sL_d}{R_d + sL_d}} & \frac{1}{sL_1 + \frac{R_d sL_d}{R_d + sL_d}} + \frac{1}{sL_2 + \frac{1}{sC_2}} + \frac{1}{sL_3} & -\frac{1}{sL_3} \\ 0 & -\frac{1}{sL_3} & \frac{1}{sL_3} + sC_4 \end{bmatrix} \cdot \begin{bmatrix} V_1 \\ V_2 \\ V_3 \end{bmatrix}$$

The system above can be solved for the node voltages, and consequently for the noise measured across the LISN resistor.

The design is complete if the noise across the LISN resistors is 6dB μ V below the limit established by the EMI standard under consideration. Otherwise, a new set of normalized parameters that provide more attenuation must be selected from Table II- 1, and steps 4 and 5 must be repeated.

Table II- 1. Normalized CC filter parameters.

Ω_s	Attenuation	L_{1n}	L_{2n}	C_{2n}	L_{3n}	C_{4n}
7.783	103	1.134	0.007212	1.391	1.983	1.258
7.297	99.14	1.132	0.009741	1.389	1.981	1.258
6.752	95.4	1.13	0.01249	1.385	1.979	1.258
6.194	91.87	1.127	0.01549	1.381	1.977	1.258
5.665	88.58	1.124	0.01879	1.377	1.975	1.259
5.198	85.54	1.12	0.02241	1.373	1.972	1.259
4.803	82.74	1.117	0.02636	1.367	1.97	1.259
4.464	80.14	1.113	0.03065	1.362	1.967	1.26
4.172	77.71	1.108	0.03528	1.356	1.964	1.26
3.916	75.44	1.104	0.04026	1.35	1.96	1.26
3.69	73.31	1.099	0.04559	1.343	1.956	1.261
3.49	71.29	1.094	0.05128	1.336	1.953	1.261
3.311	69.38	1.088	0.05734	1.328	1.949	1.262
3.151	67.56	1.082	0.06377	1.32	1.944	1.262
3.006	65.83	1.076	0.07059	1.312	1.94	1.263
2.874	64.17	1.07	0.0778	1.303	1.935	1.264
2.754	62.59	1.063	0.08542	1.294	1.93	1.264
2.644	61.06	1.056	0.09344	1.285	1.925	1.265
2.543	59.6	1.049	0.1019	1.275	1.92	1.265
2.451	58.19	1.041	0.1108	1.264	1.914	1.266
2.365	56.83	1.033	0.1201	1.253	1.908	1.267
2.286	55.51	1.025	0.1299	1.242	1.902	1.268
2.212	54.24	1.017	0.1402	1.231	1.896	1.268
2.143	53	1.008	0.151	1.219	1.89	1.269
1.47	39.9	0.8204	0.414	0.9715	1.764	1.286
1.444	36.05	0.8057	0.4383	0.9526	1.754	1.287
1.42	35.21	0.7905	0.4638	0.9334	1.745	1.288
1.397	34.38	0.775	0.4908	0.9137	1.736	1.29
1.374	33.57	0.7591	0.5193	0.8937	1.726	1.291
1.353	32.76	0.7427	0.5494	0.8733	1.716	1.292
1.333	31.97	0.7259	0.5813	0.8525	1.706	1.293
1.314	31.18	0.7087	0.6152	0.8313	1.697	1.295
1.295	30.4	0.691	0.6513	0.8097	1.687	1.296
1.278	29.63	0.6728	0.6896	0.7877	1.677	1.297
1.261	28.86	0.6542	0.7306	0.7654	1.667	1.298
1.245	28.11	0.6351	0.7744	0.7427	1.656	1.3
1.23	27.35	0.6154	0.8214	0.7197	1.646	1.301
1.215	26.6	0.5952	0.8719	0.6963	1.636	1.302
1.201	25.86	0.5745	0.9264	0.6725	1.626	1.303

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Vita



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In August of 1995, he joined the Department of Electrical Engineering of the Federal University of Paraná, Curitiba, Brazil. Since 1997, he has been with the Center for Power Electronics Systems (CPES) of Virginia Polytechnic Institute and State University. He first joined CPES as a PhD student, and in June of 2001 he became the technical director for the Center.

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